

Features

- Uses PingWei advanced PerfectMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to AEC-Q101 criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- General Automotive Applications
- Motor Drivers

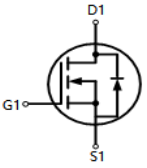
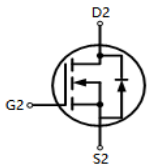
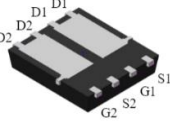
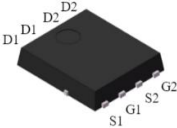


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	100V
$R_{DS(on)}@10V\ typ$	17mΩ
I_D (Silicon limit)	45A

DFN5x6双基岛



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWC210N10ESDQ	C210N10ESDQ	DFN5x6双基岛	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current $T_C = 25^{\circ}C$ (Silicon limit) $T_C = 100^{\circ}C$ (Silicon limit) $T_C = 25^{\circ}C$ (Package limit) $T_a = 25^{\circ}C$ (Note1)	I_D	45 32 40 8	A
Pulsed drain current ($T_C = 25^{\circ}C$, $t_p=100\mu s$)	$I_{D\ pulse}$	76	A
Avalanche energy, single pulse ($L=0.1mH$)	E_{AS}	9	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation $T_C = 25^{\circ}C$	P_{tot}	83	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	$^{\circ}C$
Reflow soldering temperature (10s)	T_{sold}	260	$^{\circ}C$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	-	1.8	°C/W	-
Thermal resistance, junction - ambient	RthJA	-	-	65	°C/W	1 inch ² , 2oz single copper FR-4 PCB

Electrical Characteristic (at T_j = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250uA
Gate threshold voltage	V _{GS(th)}	2	2.7	3.6	V	V _{DS} =V _{GS} , I _D =250uA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40V, V _{GS} =0V T _j =25°C T _j =125°C
Gate-source leakage current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	17	21	mΩ	V _{GS} =10V, I _D =20A

Dynamic Characteristic

Input Capacitance	C _{iss}	-	880	1408	pF	V _{GS} =0V, V _{DS} =50V, f=100KHz
Output Capacitance	C _{oss}	-	293	469		
Reverse Transfer Capacitance	C _{rss}	-	7	21		
Gate Total Charge	Q _G	-	14	22	nC	V _{DS} =50V, I _D =20A V _{GS} =10V
Gate-Source charge	Q _{gs}	-	3	7		
Gate-Drain charge	Q _{gd}	-	7	13		
Turn-on delay time	t _{d(on)}	-	8	-	ns	V _{GS} =10V, V _{DD} =50V, R _{G_ext} =1.8Ω, I _D =20A
Rise time	t _r	-	6	-		
Turn-off delay time	t _{d(off)}	-	14	-		
Fall time	t _f	-	3	-		
Gate resistance	R _G	-	1.1	3	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0V, I_{SD}=20A$
Body Diode Continuous Forward Current	I_S	-	-	45	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	76	A	$TC = 25^{\circ}C, t_p = 100\mu s$
Body Diode Reverse Recovery Time	t_{rr}	-	34	-	ns	$I_F=20A,$ $dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	29	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

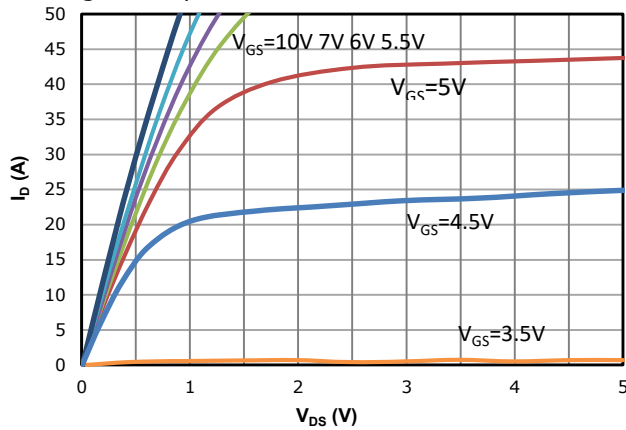


Fig 2: Transfer Characteristics

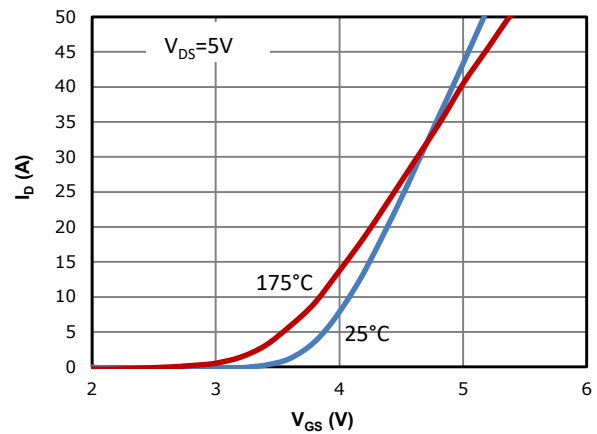


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

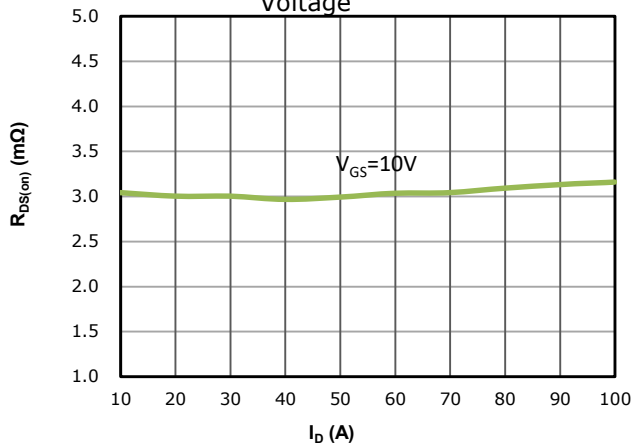


Fig 4: $R_{DS(on)}$ vs Gate Voltage

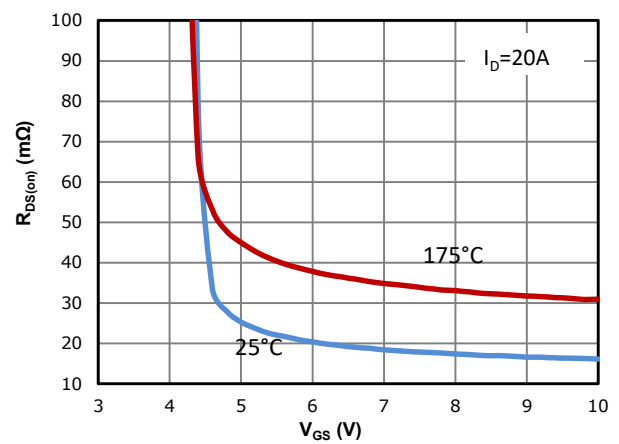


Fig 5: $R_{DS(on)}$ vs. Temperature

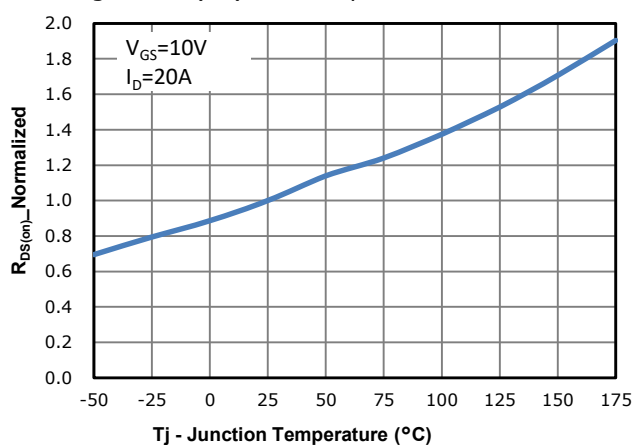


Fig 6: $V_{GS(th)}$ vs. Temperature

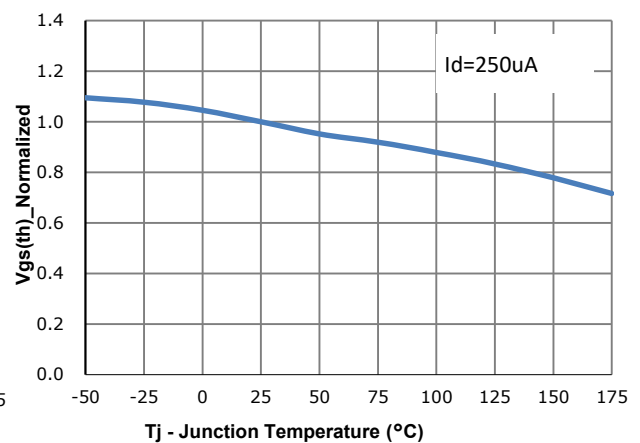


Fig 7: BVdss vs. Temperature

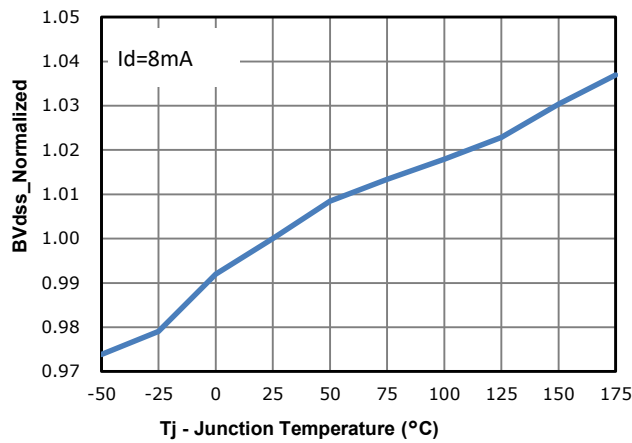


Fig 8: Capacitance Characteristics

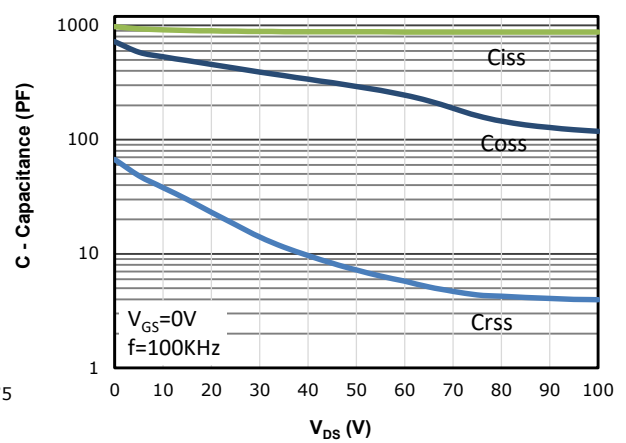


Fig 9: Gate Charge Characteristics

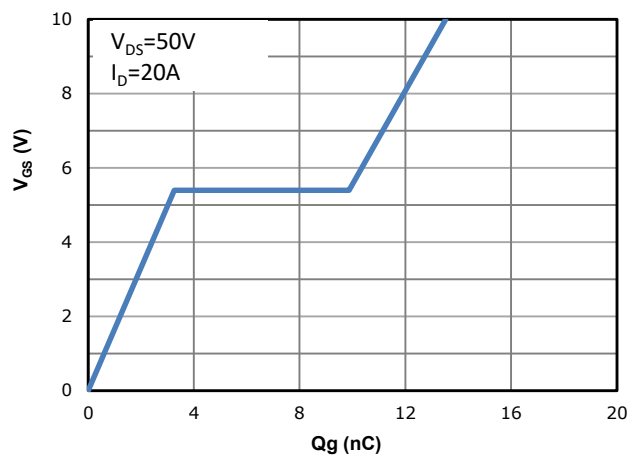


Fig 10: Body-diode Forward Characteristics

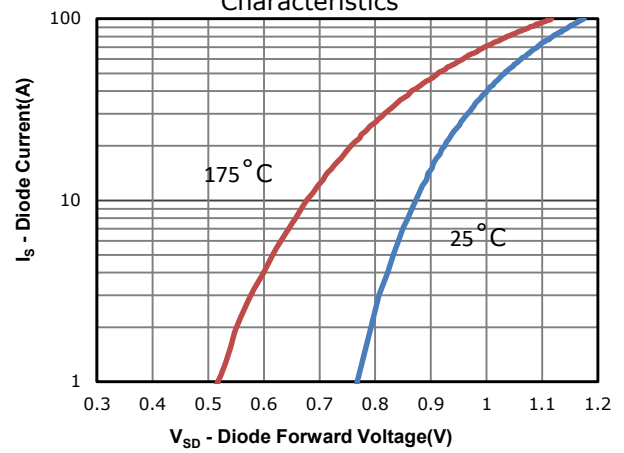


Fig 11: Power Dissipation

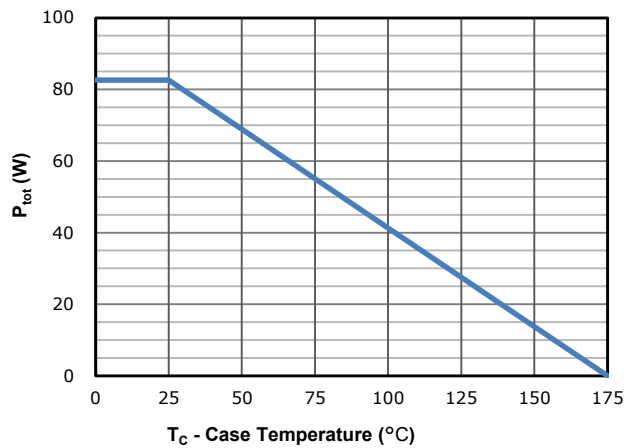


Fig 12: Drain Current Derating

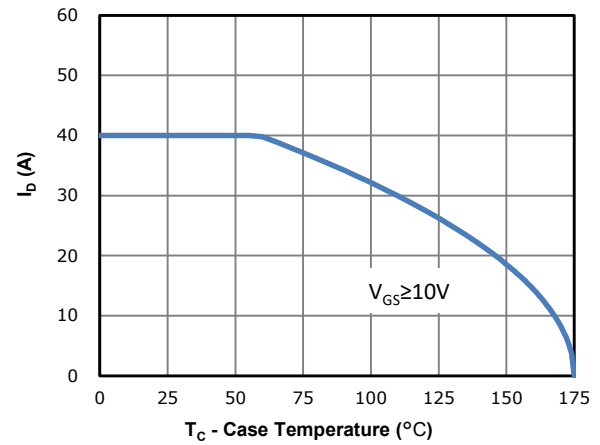


Fig 13: Safe Operating Area

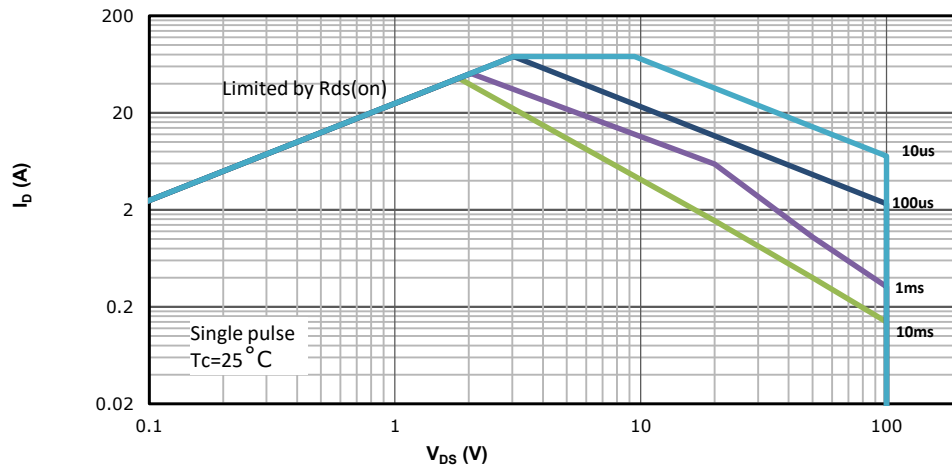
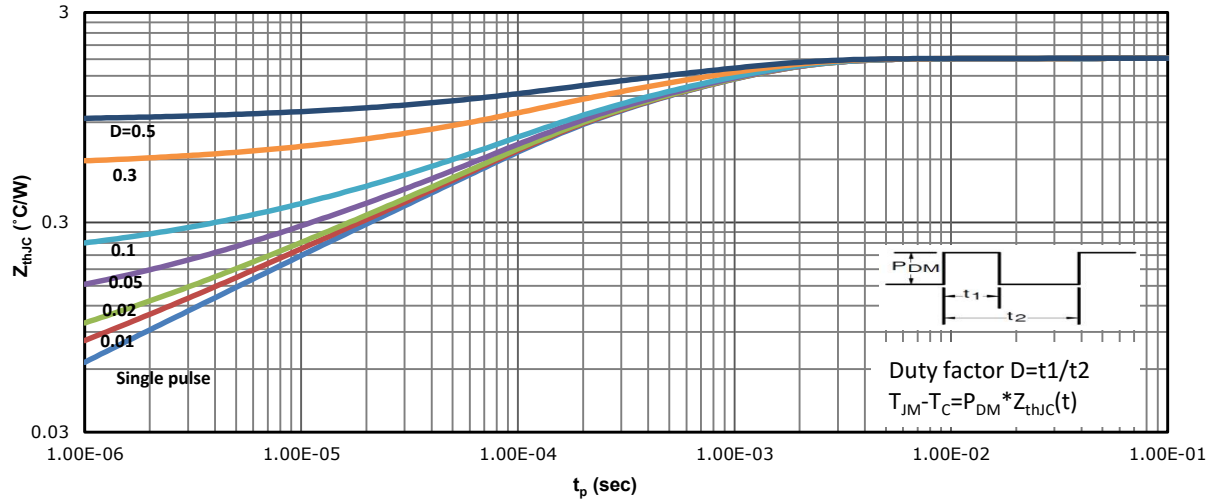
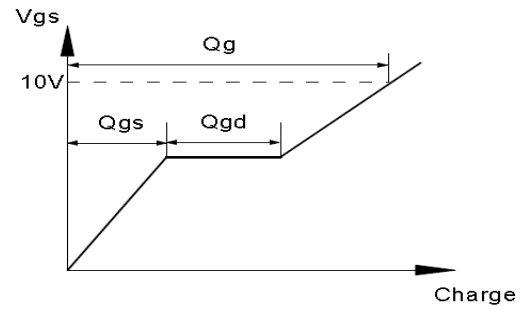


Fig 14: Max. Transient Thermal Impedance

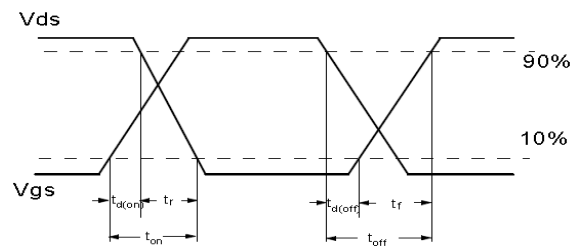


Test Circuit & Waveform

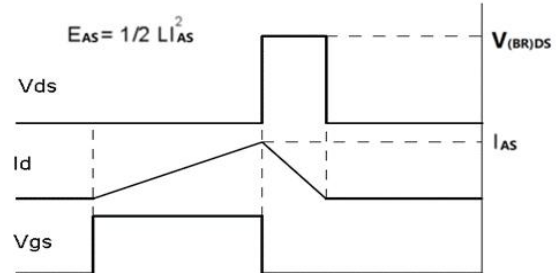
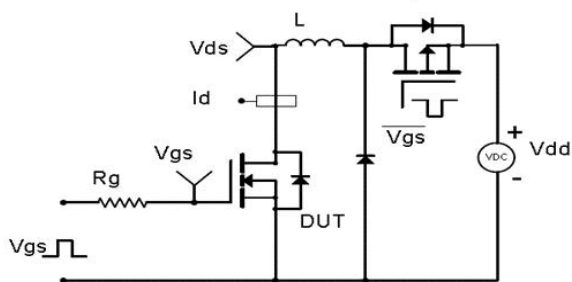
Gate Charge Test Circuit & Waveform



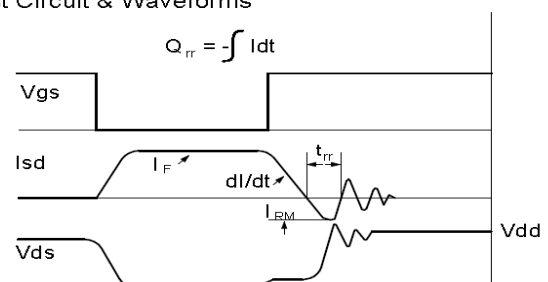
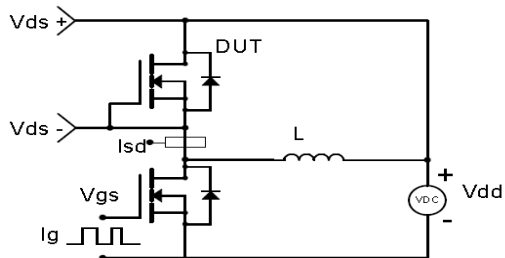
Resistive Switching Test Circuit & Waveforms

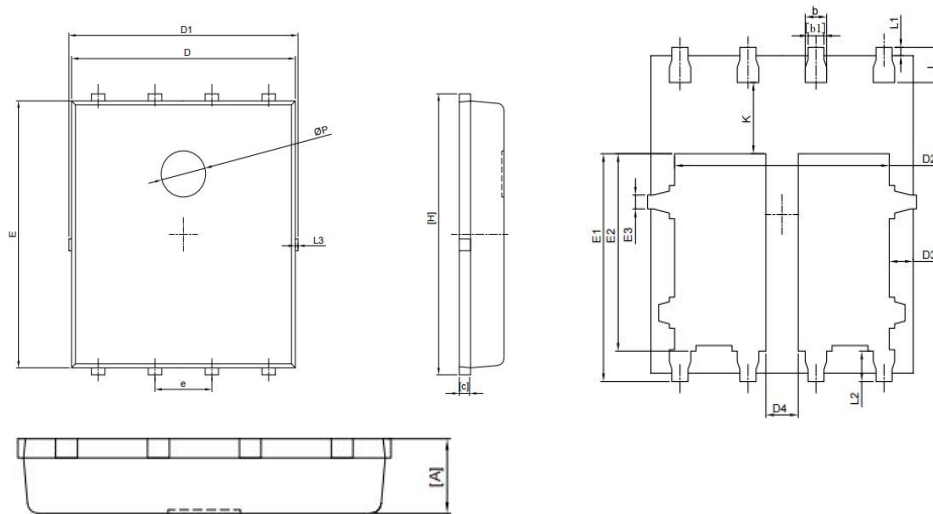


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: DFN5×6 Double Base Island Package Outline

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.30	0.50	0.012	0.020
b1	0.20	0.40	0.008	0.016
c	0.20	0.30	0.008	0.012
D	4.80	5.20	0.189	0.205
D1	5.00	5.30	0.197	0.209
D2	3.81	4.21	0.150	0.166
D3	0.24	0.64	0.009	0.025
D4	0.45	0.75	0.018	0.030
E	5.55	5.95	0.219	0.234
E1	3.88	4.38	0.153	0.172
E2	3.32	3.82	0.131	0.150
E3	0.15	0.45	0.006	0.018
e	1.27		0.050	
H	5.95	6.15	0.234	0.242
L	0.44	0.84	0.017	0.033
L1	0.05	0.25	0.002	0.010
L2	0.35	0.75	0.014	0.030
L3	-	0.22	-	0.009
K	1.09	1.49	0.043	0.059
P	0.80	1.20	0.031	0.047

Revision History

Revision	Date	Major changes
1.0	2026/2/28	Release of Formal Version
1.1	2026/6/8	Company name changed. Correct dimensions of b,b1,c,D ect.

Disclaimer

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

The product is not intended for use in applications that require extraordinary levels of quality and reliability, such as aviation/aerospace and life-support devices or systems.

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