

Features

- Uses PingWei advanced PerfectMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to AEC-Q101 criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Solid design of source leadframe

Applications

- Automotive applications
- Battery management
- Motor Drivers

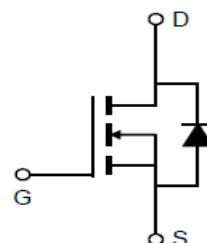
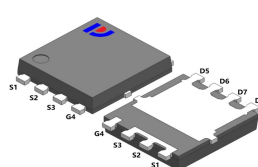


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	40V
$R_{DS(on)}@10V$ typ	1.1mΩ
I_D (Silicon limit)	252A

UPDFN5x6

**Package Marking and Ordering Information**

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWC013N04UESQ	C013N04UESQ	UPDFN5x6	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	40	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 100^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_a = 25^\circ\text{C}$ (Note1)	I_D	252 178 150 34	A
Pulsed drain current ($T_C = 25^\circ\text{C}$)	$I_{D \text{ pulse}}$	600	A
Avalanche energy, single pulse ($L=0.1\text{mH}$, $V_{ds}=32\text{V}$)	E_{AS}	268	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation $T_C = 25^\circ\text{C}$ $T_a = 25^\circ\text{C}$	P_{tot}	142 2.6	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	$^\circ\text{C}$
Reflow soldering temperature (10s)	T_{sold}	260	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	-	1.1	°C/W	-
Thermal resistance, junction - ambient	RthJA	-	-	59	°C/W	Note 1

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	2.4	2.8	3.4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	0.05	1	μA	$V_{DS}=40V, V_{GS}=0V$ $T_j=25^\circ C$ $T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	± 10	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.1	1.3	mΩ	$V_{GS}=10V, I_D=50A$
Transconductance	g_{fs}	-	109	-	S	$V_{DS}=5V, I_D=50A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	4784	7176	pF	$V_{GS}=0V, V_{DS}=20V,$ $f=250KHz$
Output Capacitance	C_{oss}	-	1628	2442		
Reverse Transfer Capacitance	C_{rss}	-	52	105		
Gate Total Charge	Q_G	-	68	137	nC	$V_{DS}=20V, I_D=50A$ $V_{GS}=10V$
Gate-Source charge	Q_{gs}	-	29	57		
Gate-Drain charge	Q_{gd}	-	8	16		
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{GS}=10V, V_{DD}=20V,$ $R_G=1.6\Omega, I_D=50A$
Rise time	t_r	-	43	-		
Turn-off delay time	$t_{d(off)}$	-	46	-		
Fall time	t_f	-	22	-		
Gate resistance	R_G	-	2.1	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Continuous Forward Current	I_S	-	-	150	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	600	A	$TC = 25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	49	-	ns	$V_R=20V, I_F=50A,$ $dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	26	-	nC	

Note1. 1 inch², 2oz single copper FR-4 PCB.

Typical Performance Characteristics

Fig 1: Output Characteristics

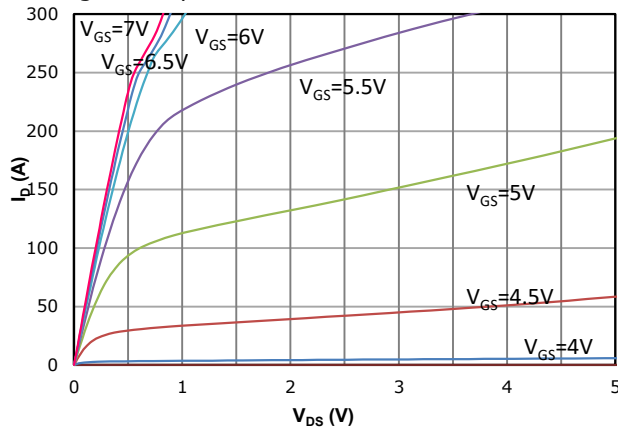


Fig 2: Transfer Characteristics

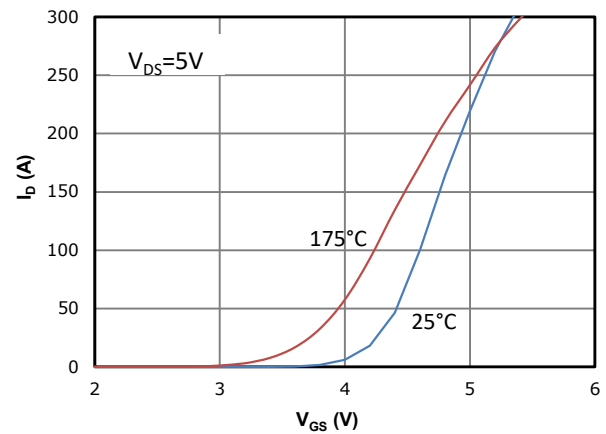


Fig 3: Rds(on) vs Drain Current and Gate Voltage

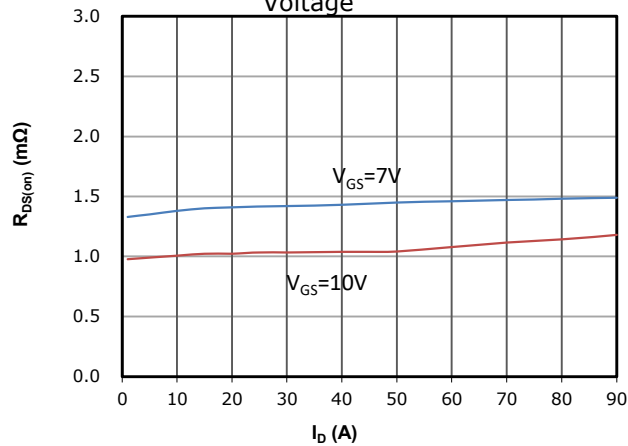


Fig 4: Rds(on) vs Gate Voltage

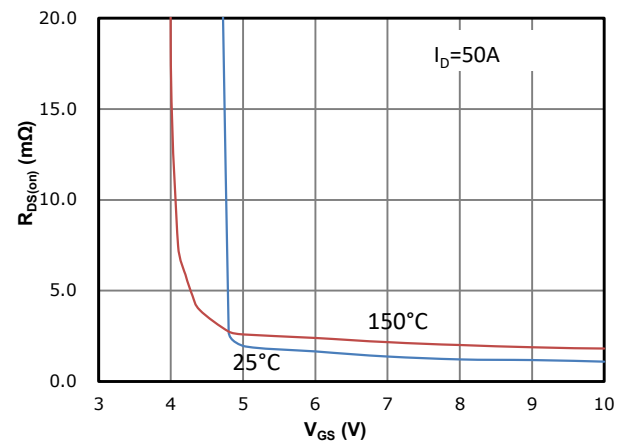


Fig 5: Rds(on) vs. Temperature

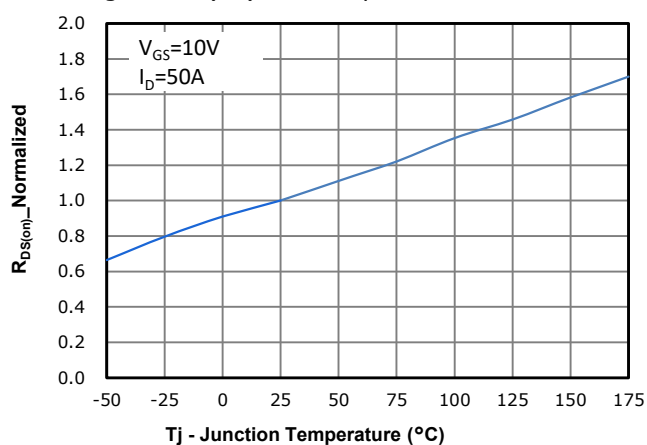


Fig 6: Vgs(th) vs. Temperature

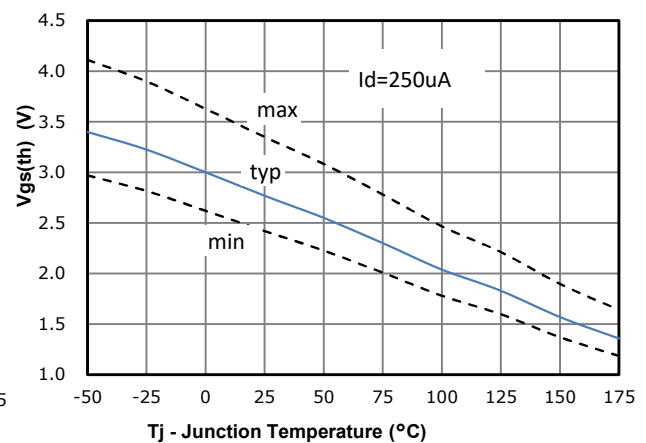


Fig 7: BVdss vs. Temperature

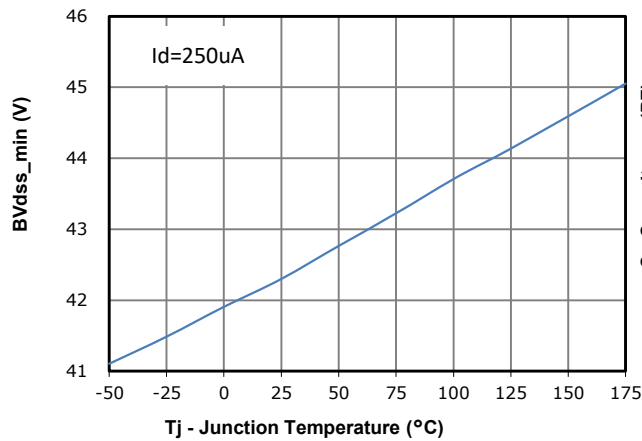


Fig 8: Capacitance Characteristics

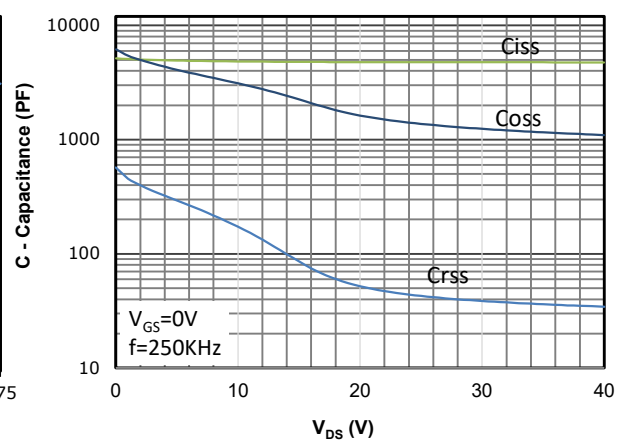


Fig 9: Gate Charge Characteristics

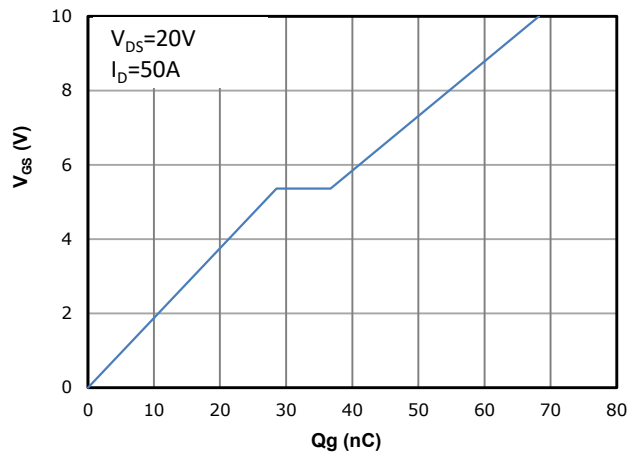


Fig 10: Body-diode Forward Characteristics

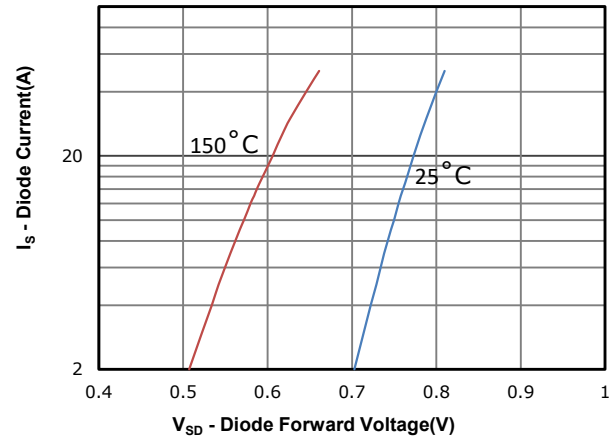


Fig 11: Power Dissipation

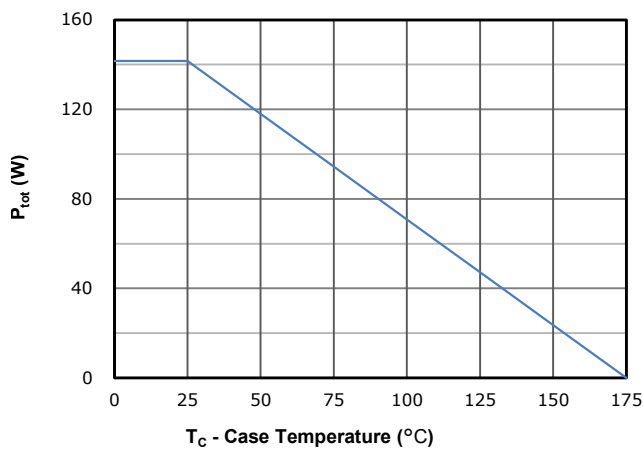


Fig 12: Drain Current Derating

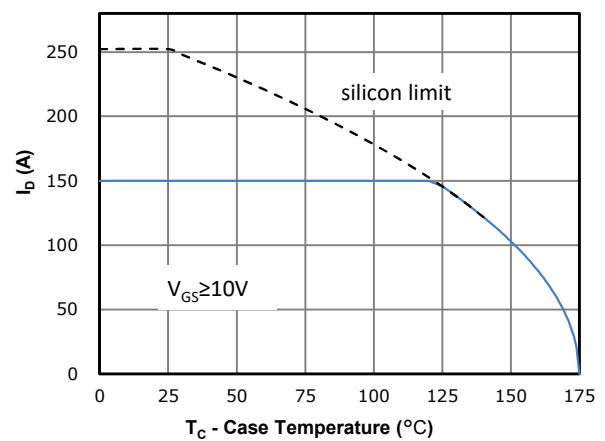


Fig 13: Safe Operating Area

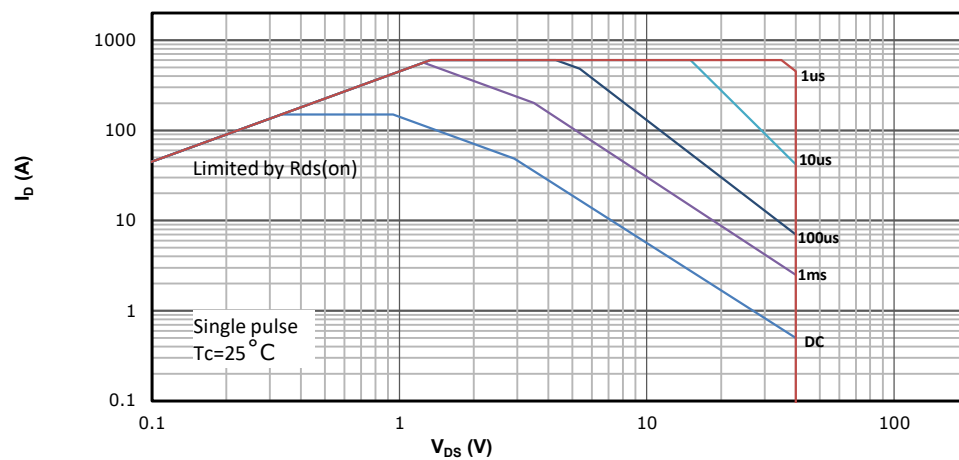
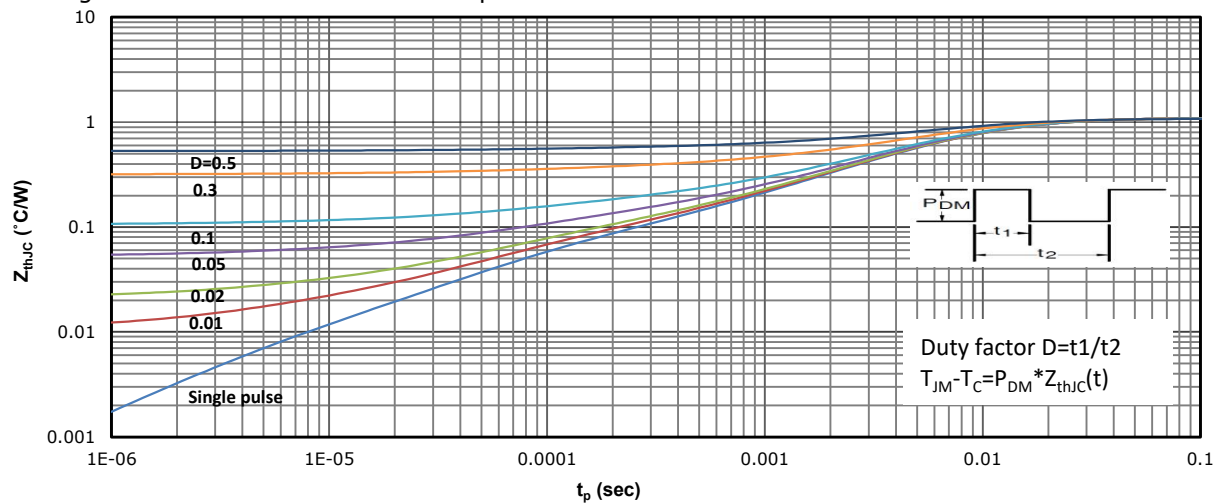
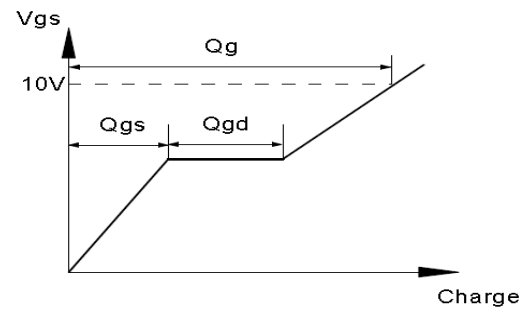
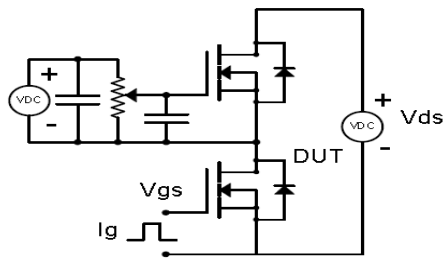


Fig 14: Max. Transient Thermal Impedance

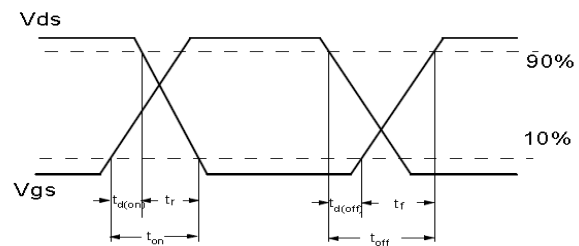
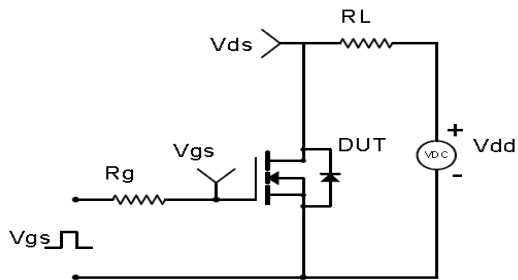


Test Circuit & Waveform

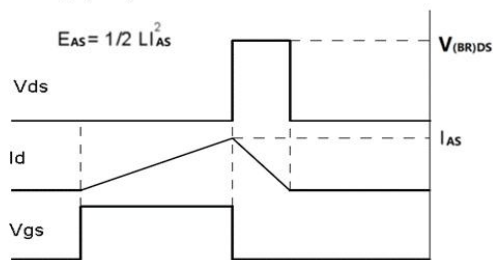
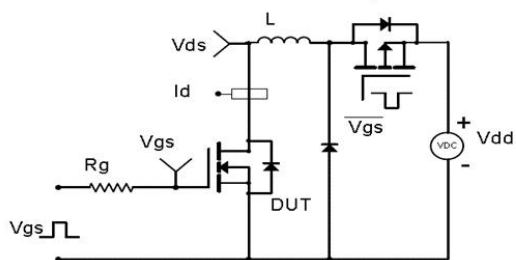
Gate Charge Test Circuit & Waveform



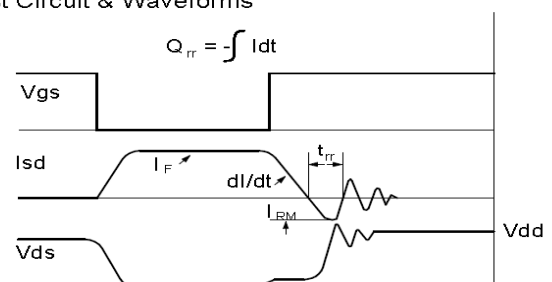
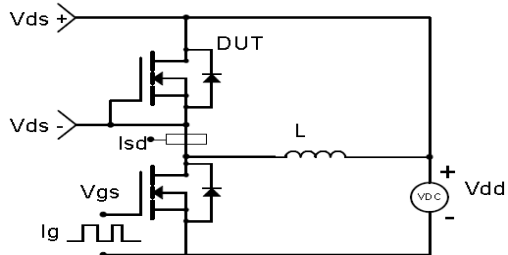
Resistive Switching Test Circuit & Waveforms

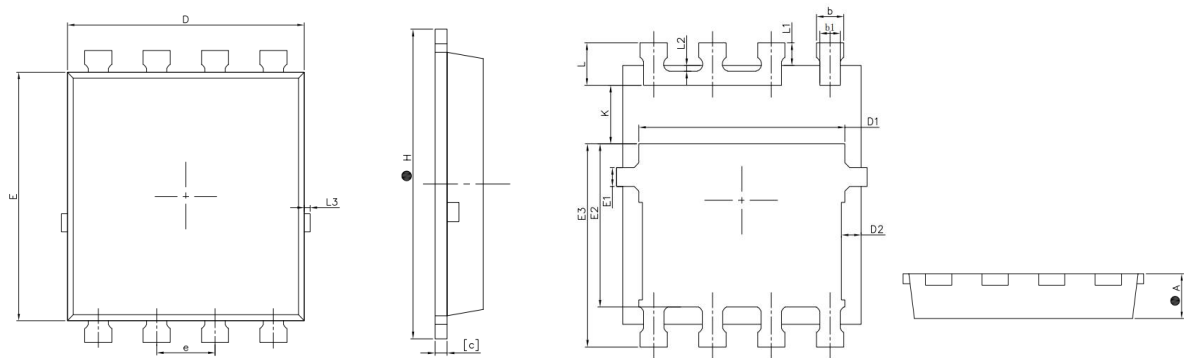


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: UPDFN5*6-C

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.49	0.69	0.019	0.027
b1	0.34	0.54	0.013	0.021
c	0.20	0.30	0.008	0.012
D	4.95	5.35	0.195	0.211
D1	4.45	4.85	0.175	0.191
D2	0.23	0.63	0.009	0.025
E	5.28	5.68	0.208	0.224
E1	0.25	0.60	0.010	0.024
E2	3.20	3.70	0.126	0.146
E3	4.05	4.55	0.159	0.179
e	1.27		0.050	
H	6.19	6.69	0.244	0.263
L	0.65	1.15	0.026	0.045
L1	0.28	0.68	0.011	0.027
L2	0.12		0.005	
L3	-	0.23	-	0.009
K	1.04	1.44	0.041	0.057

Revision History

Revision	Date	Major changes
1.0	2025/10/14	Release of Formal Version.
1.1	2025/11/18	Update EAS@L=0.1mH.
1.2	2025/12/24	Update Package Outline L2&L3.

Disclaimer

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

The product is not intended for use in applications that require extraordinary levels of quality and reliability, such as aviation/aerospace and life-support devices or systems.

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