

Features

- Enhancement mode transistor-Normally off power switch
- No reverse-recovery charge
- Low gate charge, low output charge
- Ultra high switching frequency
- Qualified according to JEDEC for target applications

Applications

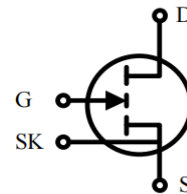
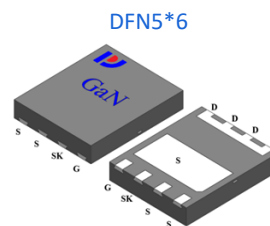
- AC-DC converters
- DC-DC converters
- Fast battery charging
- High density power conversion
- High efficiency power conversion

Benefits

- Enable very high conversion efficiencies
- Supports high operating frequency
- Enables ultrahigh power density designs
- Improved safety & reliability due to cooler operation temperature

**Product Summary**

V_{DS}	700V
$R_{DS(on)@6.0V \text{ typ.}}$	102m Ω
I_D	17A

**Package Marking and Ordering Information**

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWEG140N70E	EG140N70E	DFN5*6	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage ($T_j = -55^\circ\text{C}$ to 150°C)	V_{DSS}	700	V
Drain to source voltage transient ¹	$V_{(TR)DSS}$	800	
Drain to source voltage, pulsed ² $T_j = 25^\circ\text{C}$; total time < 10 h $T_j = 125^\circ\text{C}$; total time < 1 h	$V_{DSS,pulse}$	750	V
Continuous current, drain source	I_D	17	A
Pulsed current, drain source ³ $V_{GS} = 6V$; $T_{PULSE} = 10 \mu s$; $TC = 25^\circ\text{C}$; $V_{GS} = 6V$; $T_{PULSE} = 10 \mu s$; $TC = 125^\circ\text{C}$;	$I_{D,pulse}$	32 18	A
Gate source voltage, continuous ⁴ $T_j = -55^\circ\text{C}$ to 150°C	V_{GS}	-6~+7	V
Gate source voltage, pulsed	$V_{GS,pulse}$	-20~+10	V
Power dissipation	P_{tot}	113	W
Operating temperature	T_j	-55~+150	$^\circ\text{C}$
Storage temperature	T_{stg}		
Maximum reflow soldering temperature	T_{sold}	260	$^\circ\text{C}$

1. $V_{DSS, transient}$ is intended for non-repetitive events, $t_{PULSE} < 200 \mu s$.

2. $V_{DSS, pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100 ns$.

3. Limit was extracted from characterization test, not measured during production.

4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

Thermal Resistance

Parameter	Symbol	Limit value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – ambient	R_{thJA}	-	69	-	°C/W	-
Thermal resistance, junction - case	R_{thJC}	-	1.1	-	°C/W	-

Electrical Characteristic (at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static characteristics

Gate threshold voltage	$V_{GS(th)}$	1.2 -	1.7 1.7	2.5 -	V	$I_D = 17.2\text{mA}, V_{DS} = V_{GS}$ $T_j = 25^{\circ}\text{C}$ $T_j = 150^{\circ}\text{C}$
Drain-to-source leakage current	I_{DSS}	- -	1 7	20 -	μA	$V_{DS} = 700\text{V}, V_{GS} = 0\text{V}$ $T_j = 25^{\circ}\text{C}$ $T_j = 150^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	70	-	μA	$V_{GS} = 6\text{V}, V_{DS} = 0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	102	140	m Ω	$V_{GS} = 6\text{V}, I_D = 5\text{A}, T_j = 25^{\circ}\text{C}$
		-	210	-	m Ω	$V_{GS} = 6\text{V}, I_D = 5\text{A}, T_j = 125^{\circ}\text{C}$
Gate resistance	R_G	-	6.8	-	Ω	$f = 1\text{ MHz}; \text{ open drain}$

Dynamic characteristics

Input Capacitance	C_{iss}	-	126	-	pF	$V_{GS} = 0\text{V}, V_{DS} = 400\text{V},$ $f = 100\text{KHz}$
Output Capacitance	C_{oss}	-	47	-		
Reverse Transfer Capacitance	C_{rss}	-	1	-		
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	59	-		
Effective output capacitance, time related ²	$C_{o(tr)}$	-	82	-	nC	$V_{GS} = 0\text{V}, V_{DS} = 0\text{V} \sim 400\text{V},$
Output charge	Q_{oss}	-	33	-		
Turn-on delay time	$t_{d(on)}$	-	3	-	ns	$V_{GS} = 6\text{V}, V_{DS} = 400\text{V},$ $R_{G_on(ext)} = 10\Omega, I_D = 10\text{A},$ $R_{G_off(ext)} = 2\Omega, L = 318\mu\text{H},$ See Figure 22
Rise time	t_r	-	5	-		
Turn-off delay time	$t_{d(off)}$	-	4	-		
Fall time	t_f	-	4	-		

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Gate charge characteristics

Gate Total Charge	Q_G	-	3.5	-	nC	$V_{DS}=400V, I_D=5A$ $V_{GS}=0V-6V$
Gate-Source charge	Q_{GS}	-	0.3	-		
Gate-Drain charge	Q_{GD}	-	1.2	-		
Gate Plateau Voltage	V_{Plat}	-	2.1	-	V	$V_{DS}=400V, I_D=5A$

Reverse Device Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Source to Drain reverse Voltage	V_{SD}	-	7.8	-	V	$V_{GS}=0V, I_S=5A$
Pulsed current, reverse	$I_{S,pulse}$	-	-	32	A	$V_{GS}=6V, t_{PULSE}=10\mu s$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S=5A, V_{DS}=400V$
Reverse recovery time	t_{RR}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Typical Performance Characteristics

Fig 1: Typ. Output Characteristics

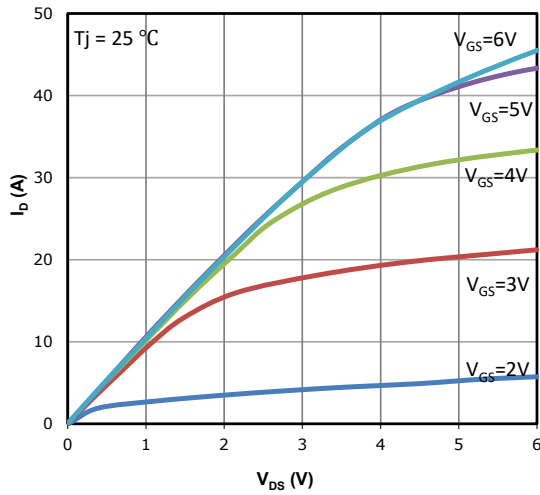


Fig 2: Typ. Output Characteristics

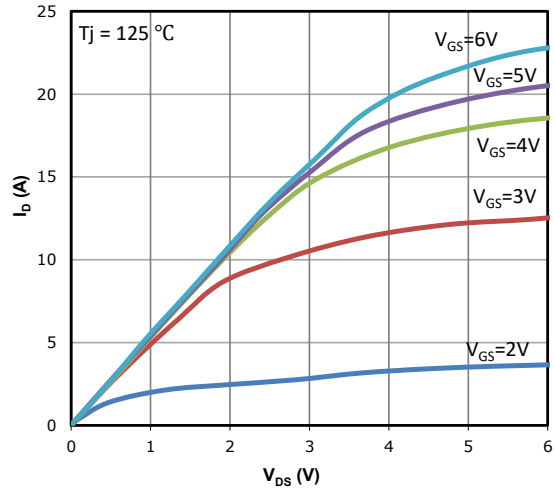


Fig 3:
Typ. Drain-source on-state resistance

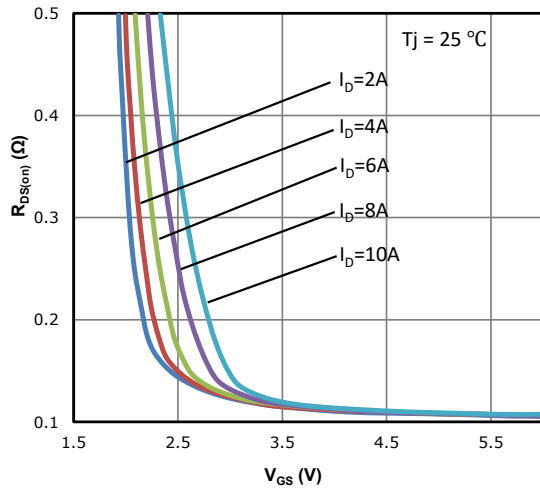


Fig 4:
Typ. Drain-source on-state resistance

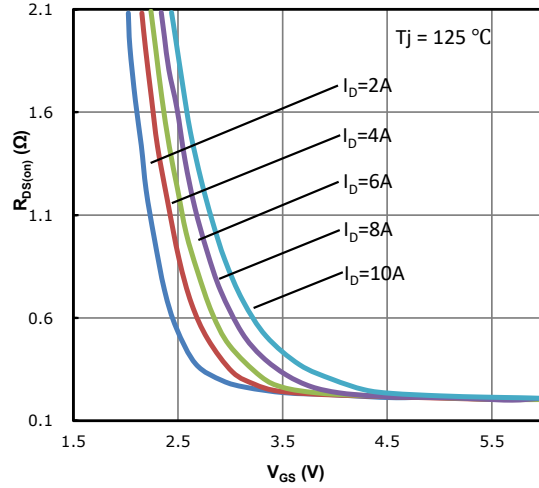


Fig 5:
Typ. channel reverse characteristics

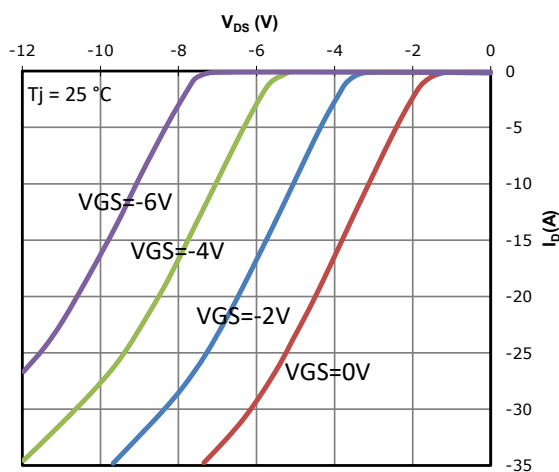


Fig 6:
Typ. channel reverse characteristics

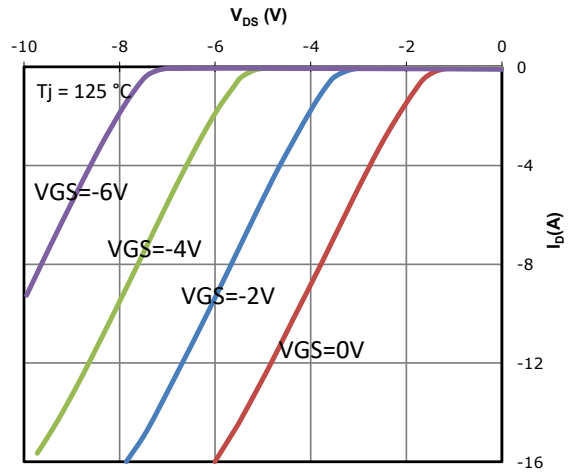


Fig 7:
Typ. channel reverse characteristics

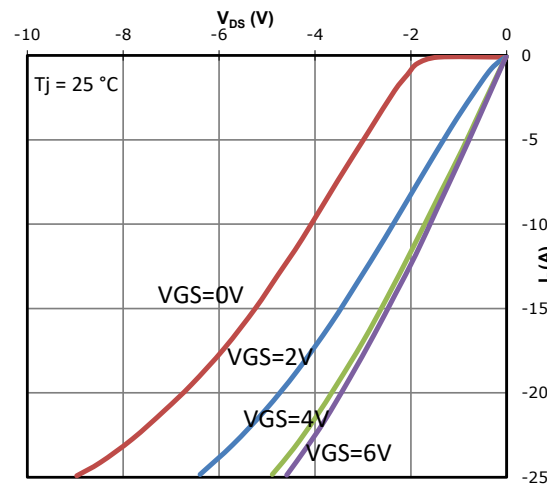


Fig 8:
Typ. channel reverse characteristics

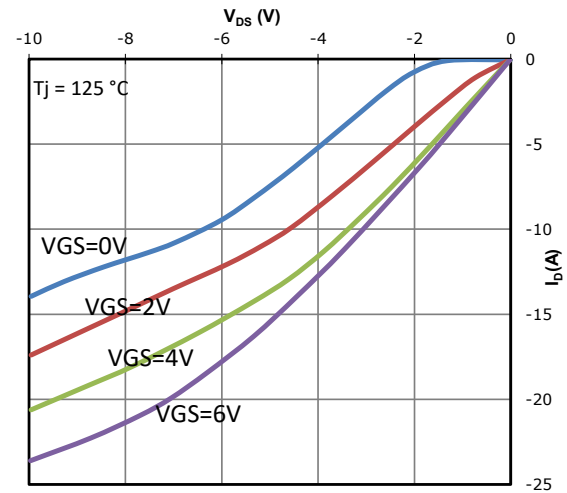


Fig 9: Typ. Transfer Characteristics

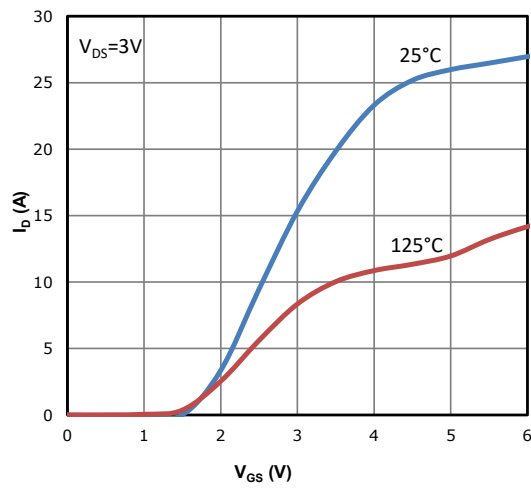


Fig 10: Typ. Gate-to-Source leakage

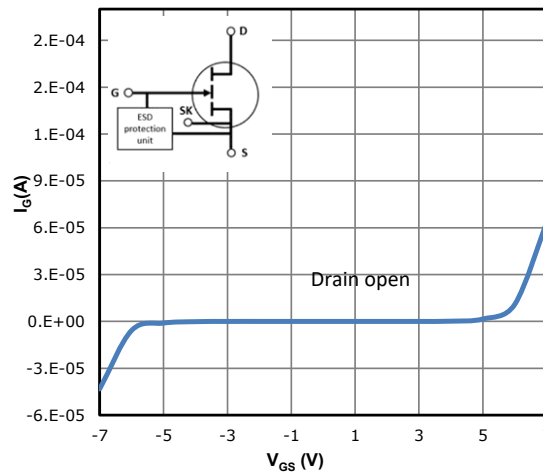


Fig 11: Drain-source leakage characteristics

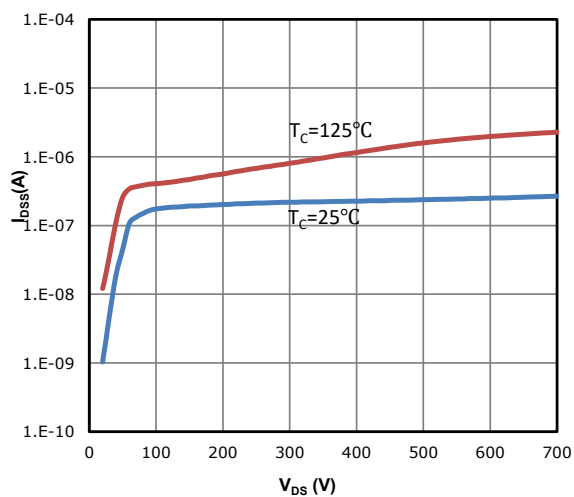


Fig 12: $V_{gs(th)}$ vs. Temperature

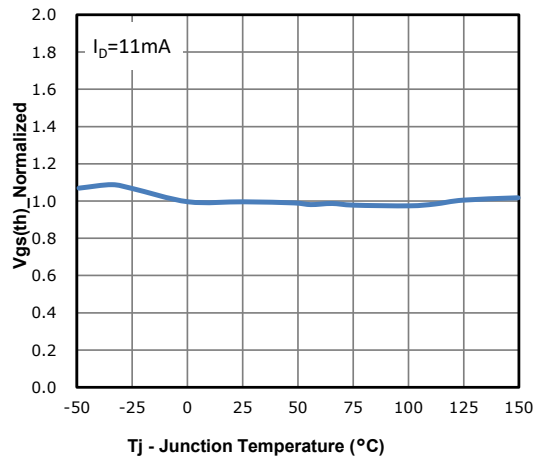


Fig 13: $R_{ds(on)}$ vs. Temperature

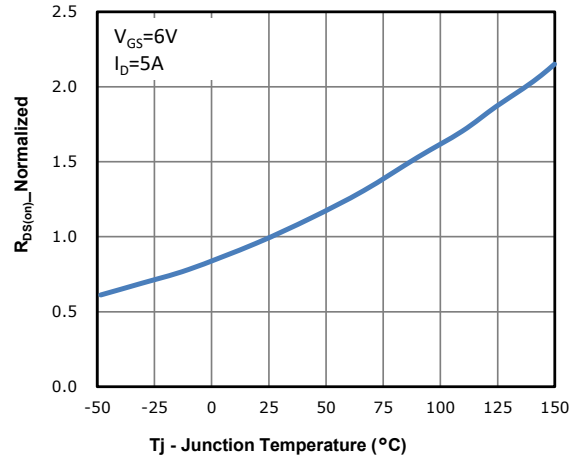


Fig 14: Power Dissipation

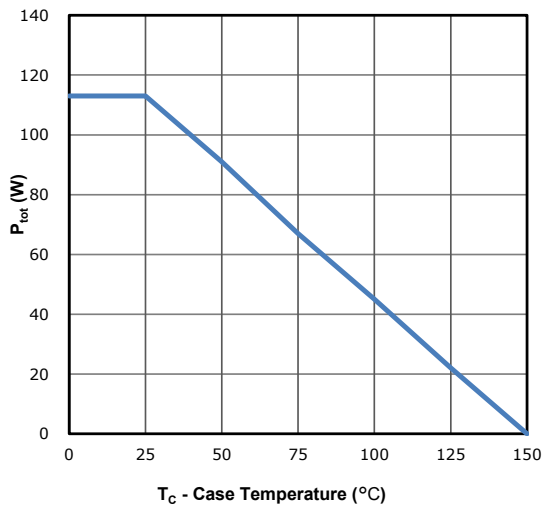


Fig 15: Max. Transient Thermal Impedance

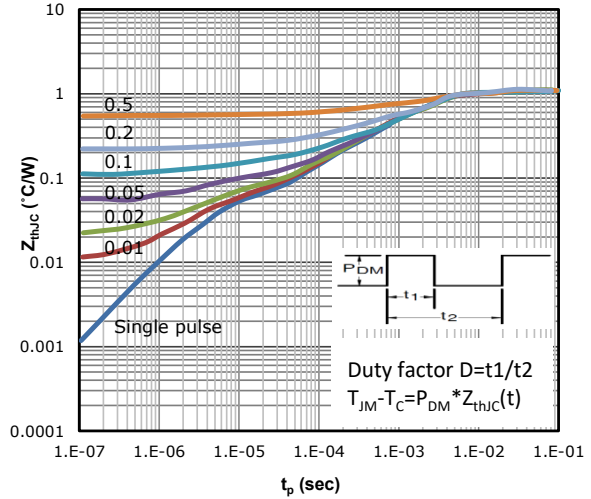


Fig 16: Safe Operating Area

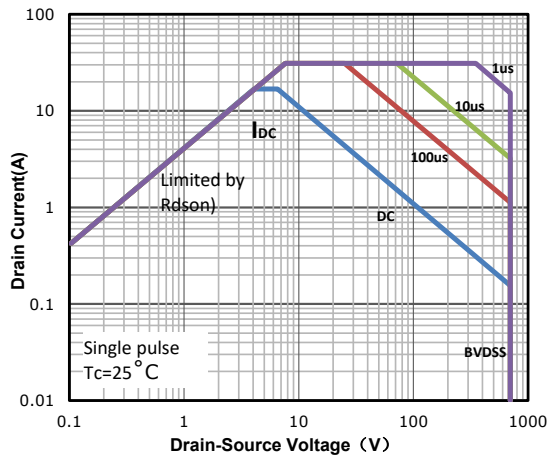


Fig 17: Safe Operating Area

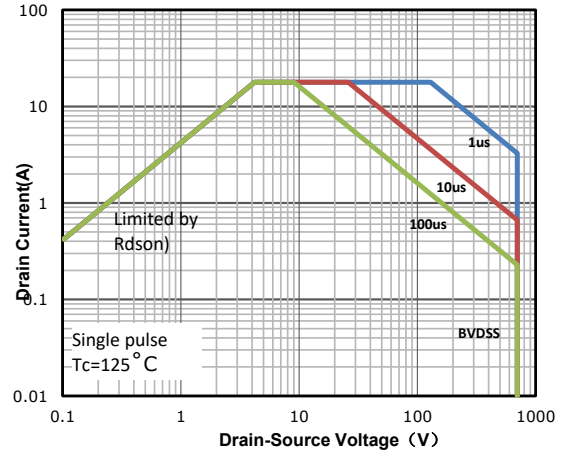


Fig 18: Gate Charge Characteristics

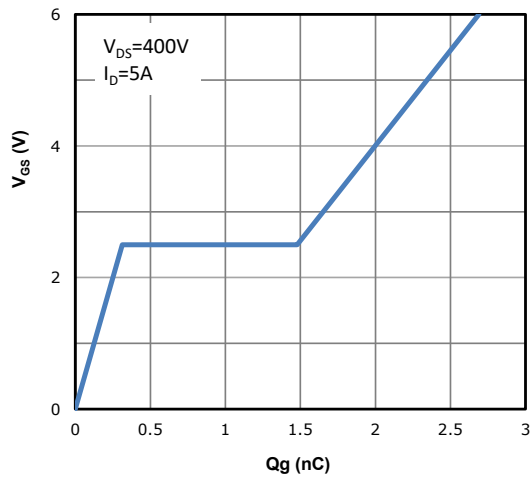


Fig 19: Capacitance Characteristics

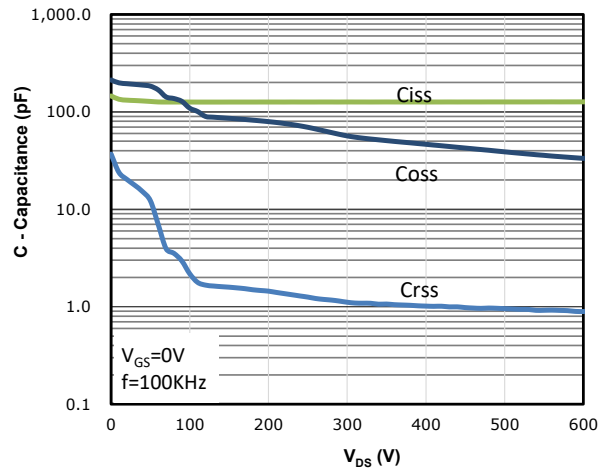


Fig 20: Typ. output charge

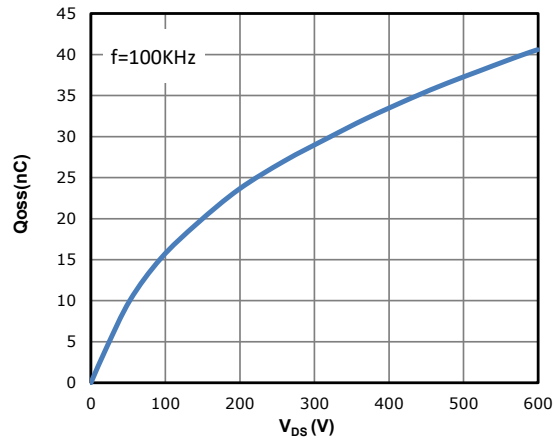
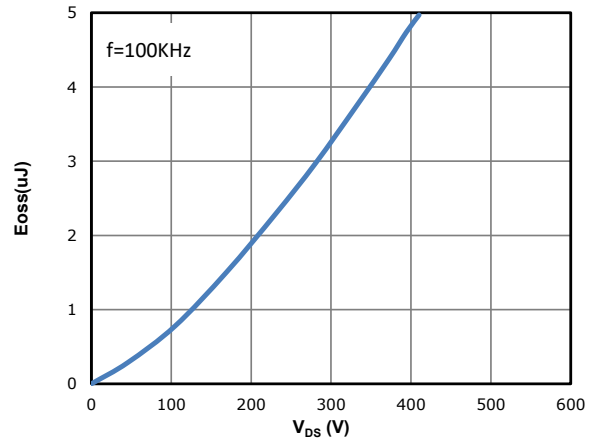
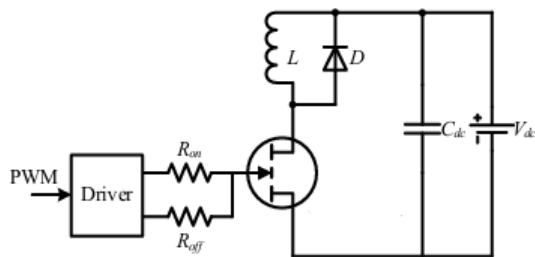


Fig 21: Typ. Coss stored Energy

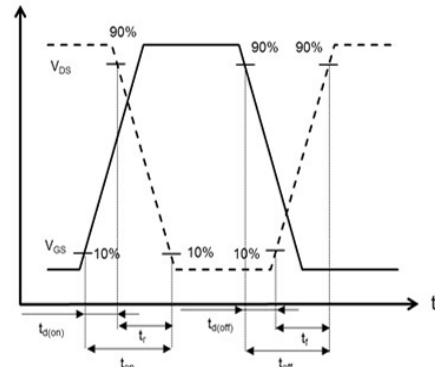


Test Circuit & Waveform

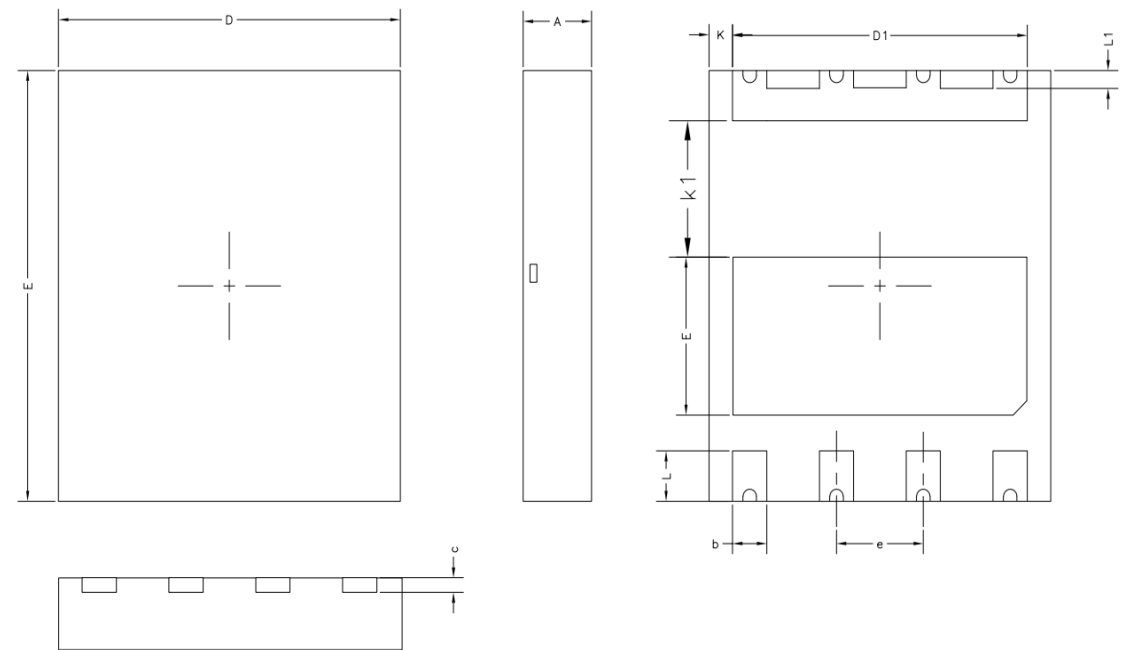
Fig 22: Typ. Switching time with inductive load Fig 23: Typ. Switching times waveform



VDS=400V, ID=6A, L=318μH,
 VGS=6V, Ron=10Ω, Roff=2Ω



Package Outline: DFN5*6



RECOMMENDED LAND PATTERN

SYMBOLS	DIMENSIONS MILLIMETERS		
	MIN	NOR	MAX
A	0.9	1.00	1.10
b	0.4	0.5	0.6
C	0.18	0.203	0.25
D	4.85	5	5.15
D1	4.16	4.31	4.46
E	5.85	6	6.15
e	1.27bsc		
L	0.55	0.7	0.85
L1	0.15	0.25	0.35
K	0.325	0.345	0.355
K1	1.70	1.90	2.10

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