

SC040N120QDQ

Silicon Carbide MOSFET 1200V, 40mΩ, 58A



重庆平伟实业股份有限公司

Features

- Low switching losses
- Extremely low on-resistance $R_{DS(on)}$
- Robust body diode operation under hard commutation events
- Easy to Parallel and Simple to Drive
- Qualified according to AEC-Q101 criteria

Applications

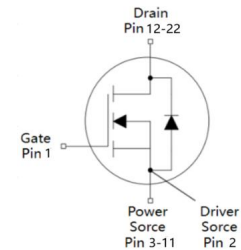
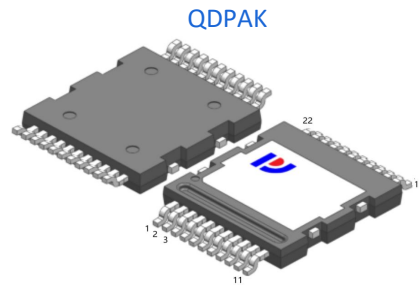
- General Automotive Applications
- On-board charger
- DC/DC converter
- Auxiliary inverters



100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	1200V
$R_{DS(on)}$ typ.	40mΩ
I_D (Silicon limit)	58A



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
SC040N120QDQ	SC040N120QDQ	QDPAK	Tape&Reel	13 inches	32mm	1000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	1200	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	58 124 41	A
Pulsed drain current ($T_C = 25^\circ\text{C}$)	$I_{D \text{ pulse}}$	232	A
Avalanche energy, single pulse ($L=5\text{mH}$)	E_{AS}	345	mJ
Gate-Source voltage,max.transient voltage	V_{GSmax}	-8/+22	V
Gate-Source voltage,max.static voltage	V_{GSsop}	-5/+18	V
Power dissipation $T_C = 25^\circ\text{C}$	P_{tot}	263	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	R_{thJC}	-	0.38	0.6	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	R_{thJA}	-	-	66	°C/W	-

Electrical Characteristic (at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	1200	-	-	V	$V_{GS}=0V, I_D=100\mu A$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.4	4.2	V	$V_{DS}=V_{GS}, I_D=10mA$
Zero gate voltage drain current	I_{DSS}	-	1	10	μA	$V_{DS}=1200V, V_{GS}=0V$ $T_j=25^{\circ}C$ $T_j=175^{\circ}C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=22V, V_{DS}=0V$
		-	-	-100	nA	$V_{GS}=-8V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	40	52	mΩ	$V_{GS}=18V, I_D=40A$
Transconductance	g_{fs}	-	18	-	S	$V_{DS}=20V, I_D=20A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	2132	-	pF	$V_{GS}=0V, V_{DS}=800V,$ $f=1MHz$
Output Capacitance	C_{oss}	-	108	-		
Reverse Transfer Capacitance	C_{rss}	-	5	-		
Gate Total Charge	Q_G	-	98	-	nC	$V_{DS}=800V, I_D=33A$ $, V_{GS}=-5V/18V$
Gate-Source charge	Q_{gs}	-	33	-		
Gate-Drain charge	Q_{gd}	-	33	-		
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{GS}=-5/18V,$ $V_{DD}=800V,$ $R_G=5\Omega, I_D=33A$
Rise time	t_r	-	13	-		
Turn-off delay time	$t_{d(off)}$	-	25	-		
Fall time	t_f	-	9	-		
Gate resistance	R_G	-	1.4	-	Ω	$V_{GS}=0V, f=1MHz$

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	3.3	-	V	$V_{GS} = -5V, I_{SD} = 20A$ $T_j = 25^{\circ}C$
		-	3.0	-		$T_j = 175^{\circ}C$
Body Diode Continuous Forward Current	I_S	-	-	58	A	$T_C = 25^{\circ}C$
		-	-	41	A	$T_C = 100^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	16	-	ns	$V_{GS} = -5V, I_{SD} = 33A,$ $V_R = 800V$ $di/dt = 1200A/us$
Body Diode Reverse Recovery Charge	Q_{rr}	-	121	-	nC	
Peak Reverse Recovery Current	I_{RRM}	-	13	-	A	

Typical Performance Characteristics

Fig 1: Output Characteristics $T_j=25^\circ\text{C}$

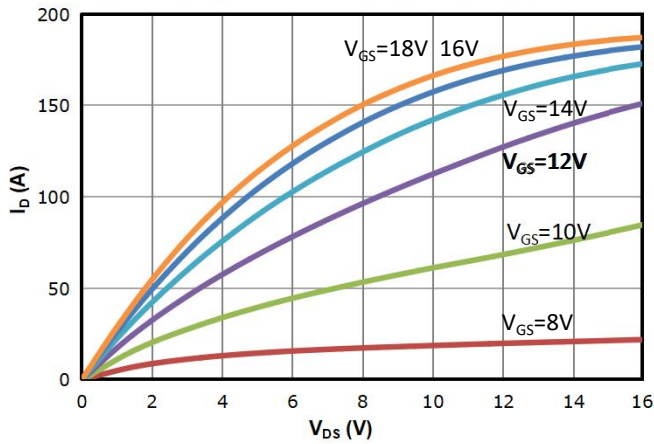


Fig 2: Output Characteristics $T_j=175^\circ\text{C}$

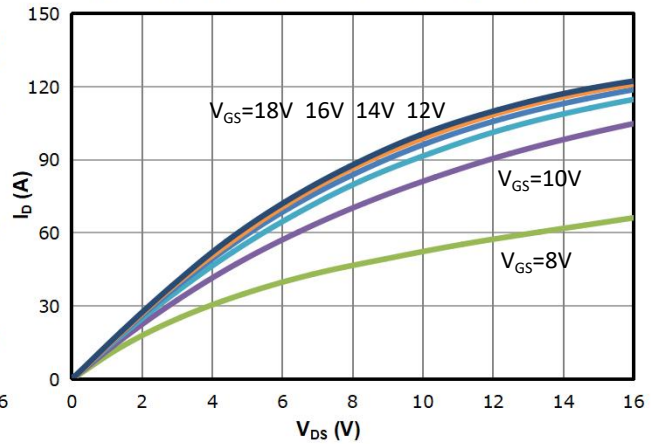


Fig 3: Transfer Characteristics

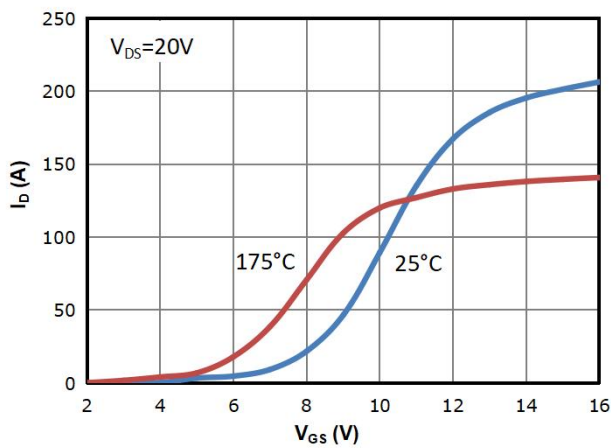


Fig 4: $R_{DS(on)}$ vs Drain Current and Gate Voltage

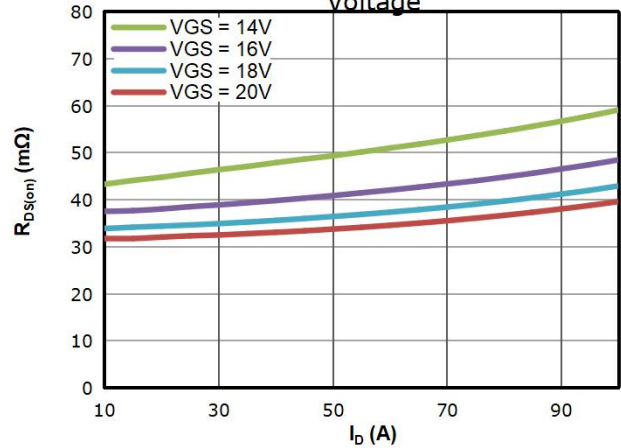


Fig 5: $R_{DS(on)}$ vs. Temperature

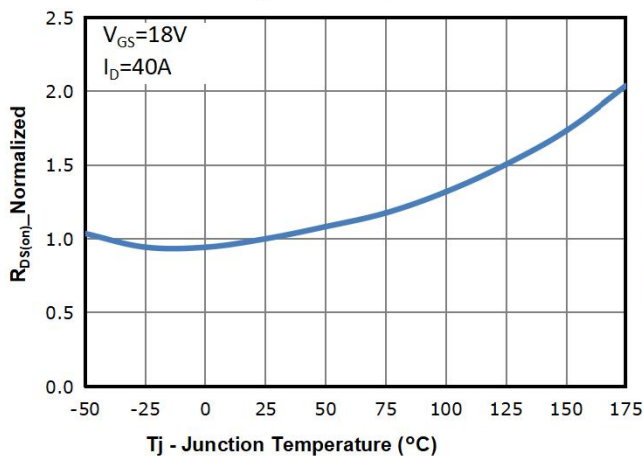


Fig 6: $V_{GS(th)}$ vs. Temperature

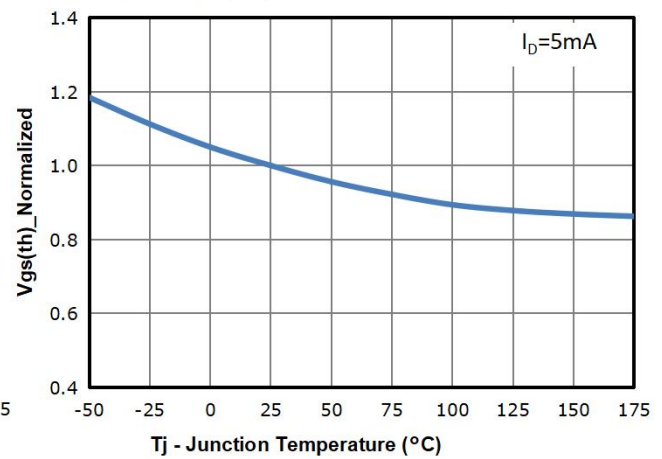


Fig 7: BVdss vs. Temperature

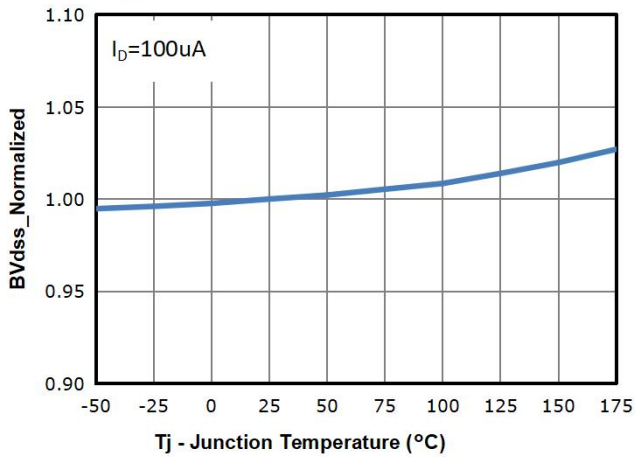


Fig 8: Capacitance Characteristics

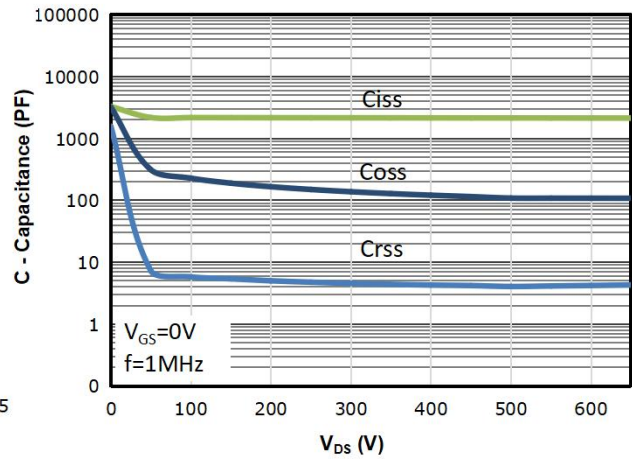


Fig 9: Gate Charge Characteristics

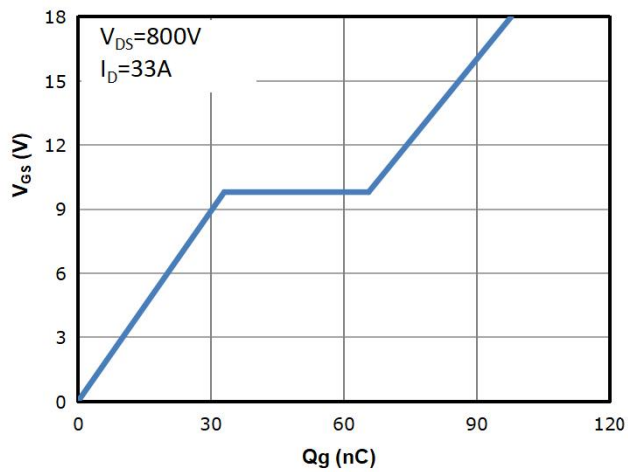


Fig 10: Body-diode Forward Characteristics

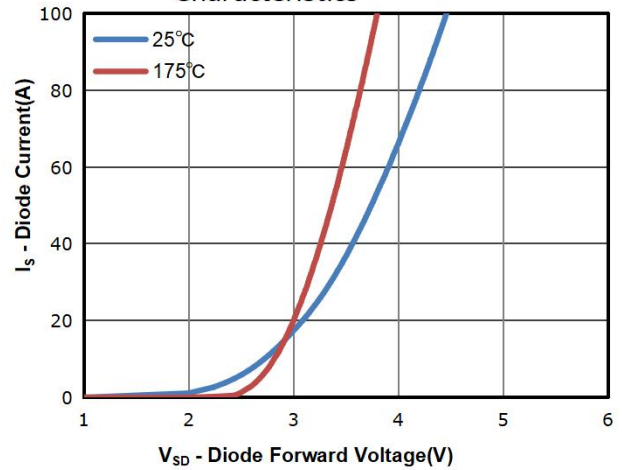


Fig 11: Power Dissipation

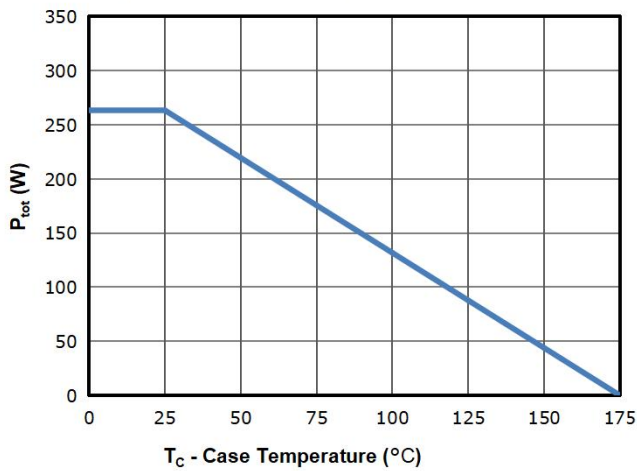


Fig 12: Drain Current Derating

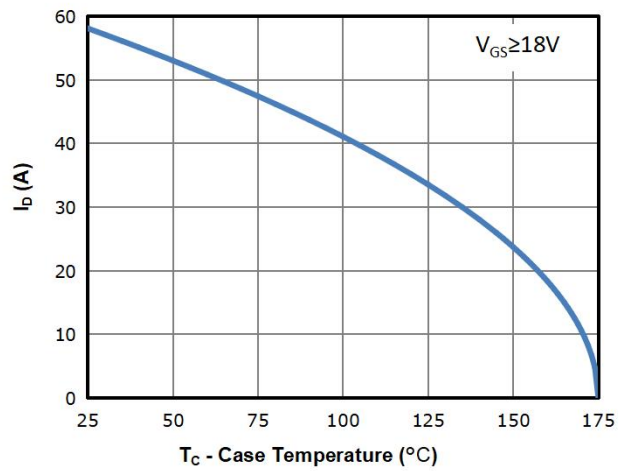


Fig 13: Safe Operating Area

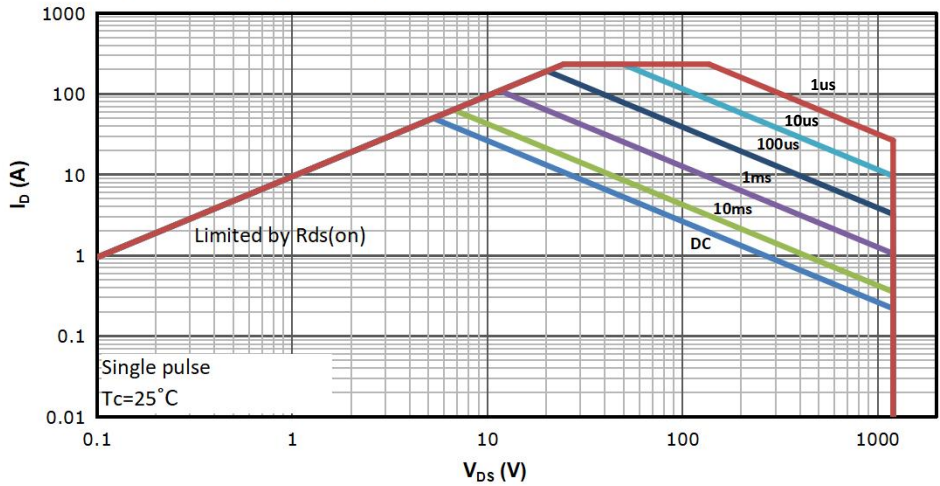
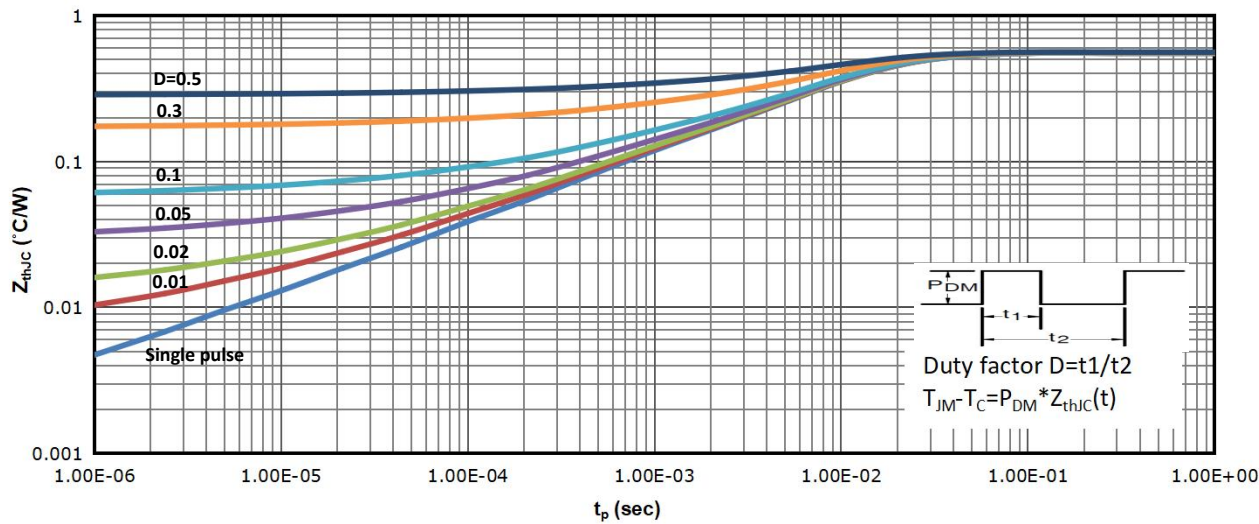
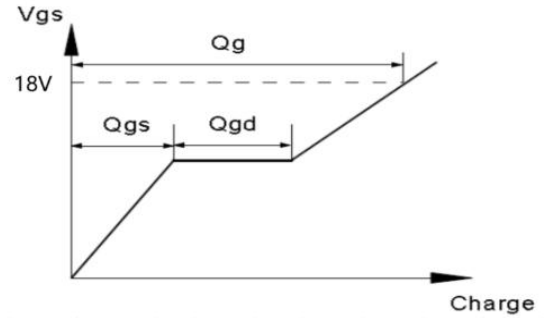
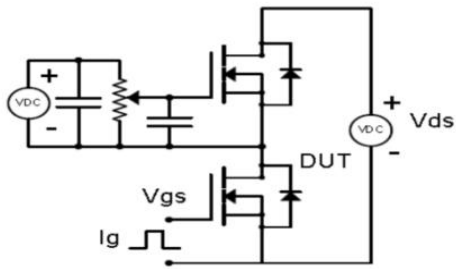


Fig 14: Max. Transient Thermal Impedance

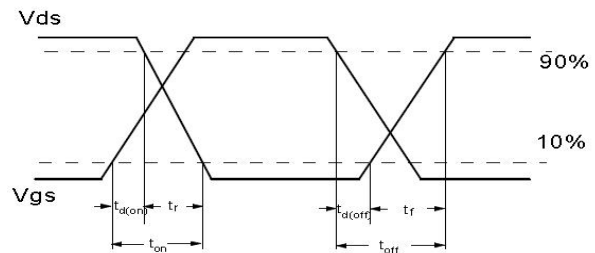
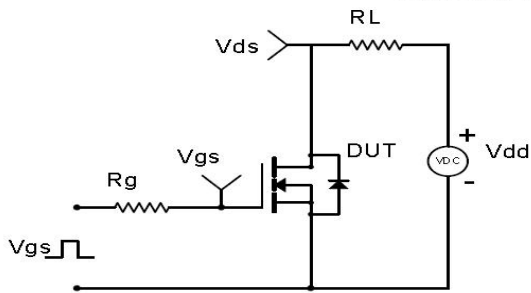


Test Circuit & Waveform

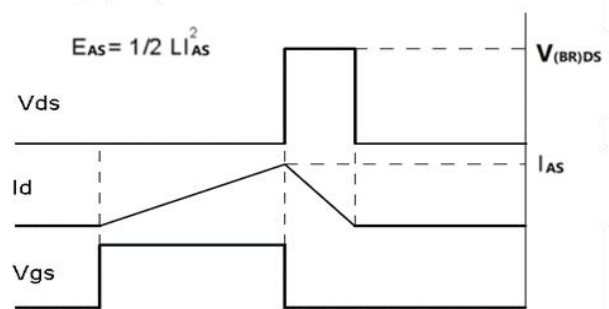
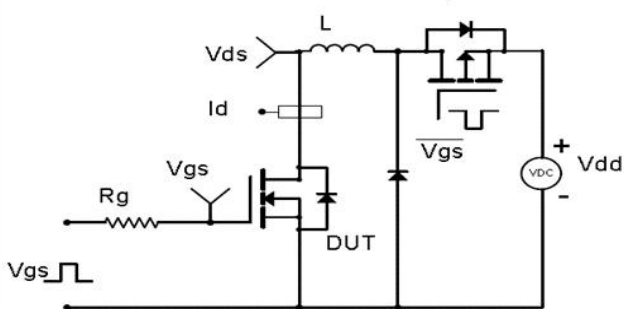
Gate Charge Test Circuit & Waveform



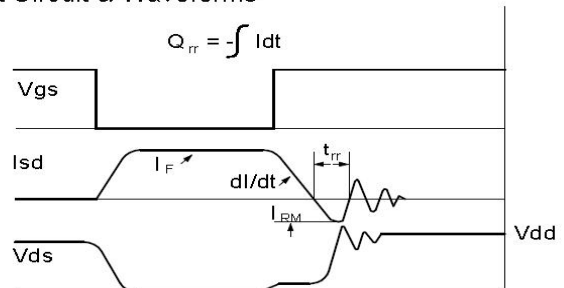
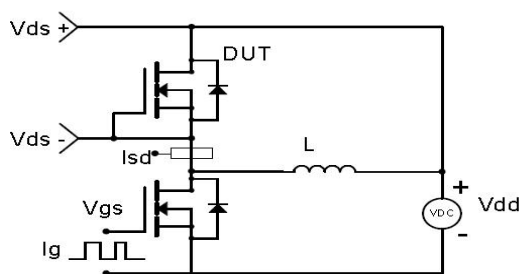
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



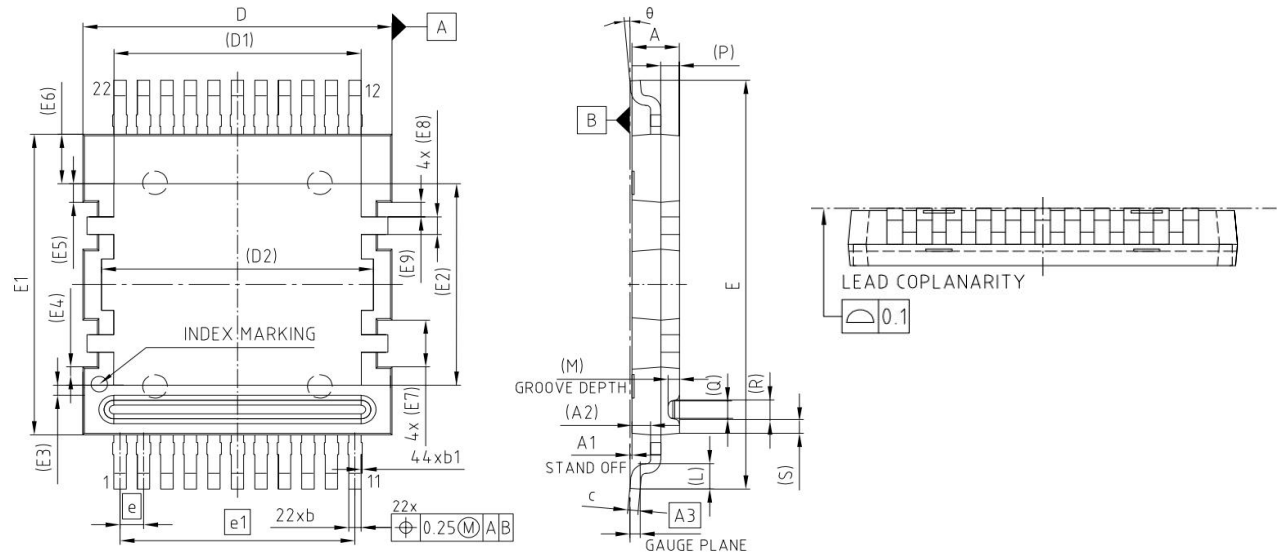
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Package Outline: QDPAK



DIMENSIONS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.25	2.35	0.089	0.093
A1	0.00	0.15	0.000	0.006
A2	0.90		0.035	
A3	0.50		0.020	
b	0.50	0.70	0.020	0.028
b1	---	0.15	---	0.006
c	0.46	0.58	0.018	0.023
D	14.90	15.10	0.587	0.594
D1	12.00		0.472	
D2	13.20		0.520	
E	20.81	21.11	0.819	0.831
E1	15.30	15.50	0.602	0.610
E2	10.32		0.406	
E3	0.625		0.025	
E4	0.45		0.018	
E5	0.95		0.037	
E6	2.53		0.100	
E7	2.40		0.094	
E8	0.90		0.035	
E9	0.75		0.030	
e	1.14		0.045	
e1	11.4		0.449	
L	1.30		0.051	
M	0.55		0.022	
θ	0°	8°	0°	8°
P	0.90		0.035	
Q	0.94		0.037	
R	1.12		0.044	
S	0.66		0.026	

Revision History

Revision	Date	Major changes
1.0	2025/8/11	Release of Formal Version

Disclaimer

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

The product is not intended for use in applications that require extraordinary levels of quality and reliability, such as aviation/aerospace and life-support devices or systems.

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