PWEG245N70E

PW 700V GaN HEMT

重庆平伟实业股份有限公司

Features

- Enhancement mode transistor-Normally off power switch
- No reverse-recovery charge
- Low gate charge, low output charge
- Ultra high switching frequency
- Qualified according to JEDEC for target applications

Applications

- AC-DC converters
- DC-DC converters
- Fast battery charging
- High density power conversion
- High efficiency power conversion

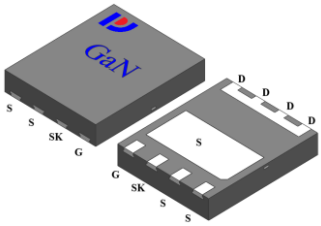
Benefits

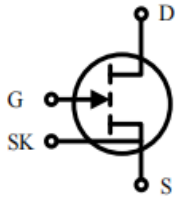
- Enable very high conversion efficiencies
- Supports high operating frequency
- Enables ultrahigh power density designs
- Improved safety & reliability due to cooler operation temperature

Product Summary

V_{DS}	700V
$R_{DS(on)@6.0V\ typ.}$	190mΩ
I_D	10A

DFN5*6





Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWEG245N70E	EG245N70E	DFN5*6	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage（T_j=-55 °Cto 150°C）	V_{DSS}	700	V
Drain to source voltage transient[1]	$V_{(TR)DSS}$	800	
Drain to source voltage,pulsed[2] T_j = 25 °C; total time < 10 h T_j = 125 °C; total time < 1 h	$V_{DSS,pulse}$	750	V
Continuous current, drain source	I_D	10	A
Pulsed current, drain source[3] T_C = 25°C； V_{GS} = 6V t_{PULSE} = 10 μs	$I_{D,pulse}$	18 10	A
Gate source voltage, continuous[4] T_j=-55°C to 150°C	V_{GS}	-1~7	V
Gate source voltage, pulsed	$V_{GS,pulse}$	-20~10	V
Power dissipation	P_{tot}	75	W
Operating temperature	T_j	-55~150	°C
Storage temperature	T_{stg}		
Maximum reflow soldering temperature	T_{sold}	260	°C

1.$V_{DS,\ transient}$ is intended for non-repetitive events, t_{PULSE} < 200 μs.
2.$V_{DS,\ pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.
3.Limit was extracted from characterization test, not measured during production.
4.The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

Thermal Resistance

Parameter	Symbol	Limit value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – ambient	R_{thJA}	-	70	-	°C/W	-
Thermal resistance, junction - case	R_{thJC}	-	1.66	-	°C/W	-

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static characteristics						
Gate threshold voltage	$V_{GS(th)}$	1.2 -	1.4 1.4	2.5 -	V	I_D=11mA,V_{DS}=V_{GS} Tj=25°C Tj=150°C
Drain-to-source leakage current	I_{DSS}	- -	0.2 5	10 -	μA	V_{DS}=700V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	5	-	μA	V_{GS}=6V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	190	245	mΩ	V_{GS}=6V,Id=3A,T_J=25°C
		-	408	-	mΩ	V_{GS}=6V,I_D=3A,T_J=125°C
Gate resistance	R_G	-	1.1	-	Ω	f = 1 MHz; open drain
Dynamic characteristics						
Input Capacitance	C_{iss}	-	63	-	pF	V_{GS}=0V, V_{DS}=400V, f=100KHz
Output Capacitance	C_{oss}	-	15	-		
Reverse Transfer Capacitance	C_{rss}	-	0.7	-		
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	40	-		V_{GS}=0V, V_{DS}=0V~400V,
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	50	-		
Output charge	Q_{OSS}	-	19	-	nC	
Turn-on delay time	$t_{d(on)}$	-	3	-	ns	V_{GS}=6V, V_{DS}=400V, $R_{G\_on(ext)}$=10Ω,I_D=6A, $R_{G\_off(ext)}$=2Ω, L=318μH, See Figure 22
Rise time	t_r	-	4	-		
Turn-off delay time	$t_{d(off)}$	-	3	-		
Fall time	t_f	-	3	-		

1.$C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2.$C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Gate charge characteristics

Gate Total Charge	Q_G	-	2.5	-	nC	V_{DS}=400V,I_D=3A ,V_{GS}=0V-6V
Gate-Source charge	Q_{GS}	-	0.4	-		
Gate-Drain charge	Q_{GD}	-	1	-		
Gate Plateau Voltage	V_{Plat}	-	2.5	-	V	V_{DS}=400V,I_D=3A

Reverse Device Characteristic

Parameter	**Symbol**	**Value**			**Unit**	**Test Condition**
		min.	**typ.**	**max.**		
Source to Drain reverse Voltage	V_{SD}	-	5	-	V	V_{GS}=0V,I_{SD}=3A
Pulsed current, reverse	$I_{S,pulse}$	-	-	18	A	V_{GS}=6V,t_{PULSE}=10μs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S=3A,V_{DS}=400V
Reverse recovery time	t_{RR}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Typical Performance Characteristics

Fig 1: Typ. Output Characteristics

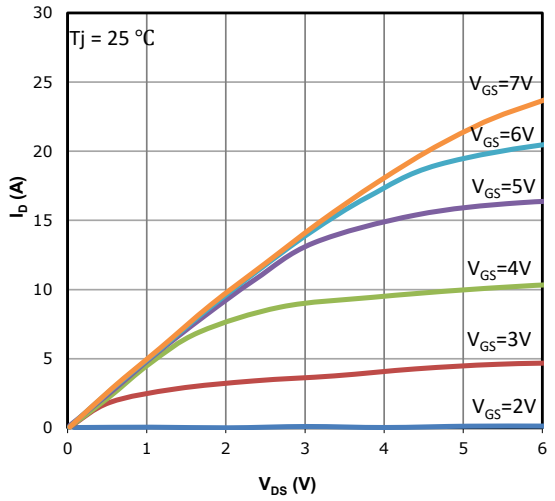


Fig 2: Typ. Output Characteristics

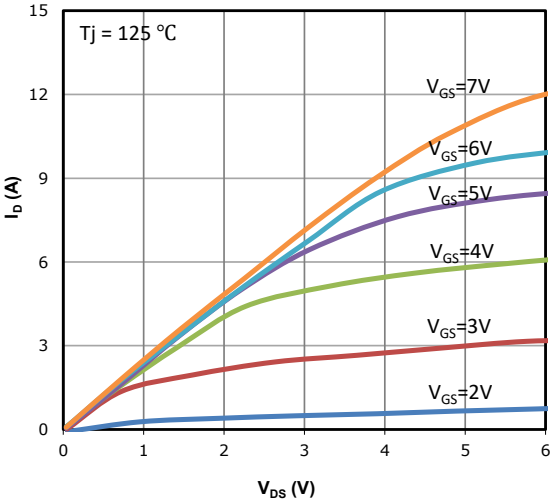


Fig 3:
Typ.Drain-source on-state resistance

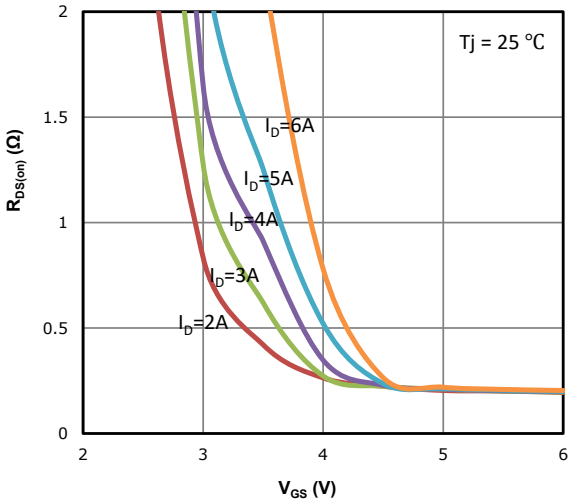


Fig 4:
Typ.Drain-source on-state resistance

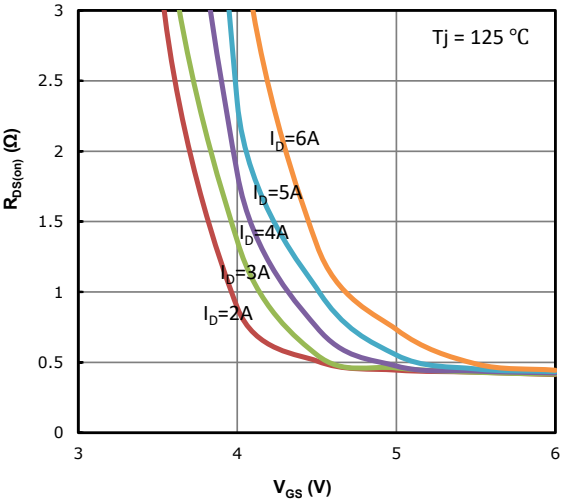


Fig 5:
Typ. channel reverse characteristics

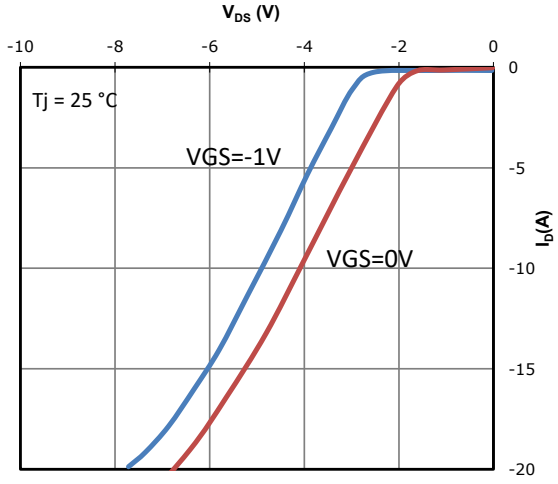


Fig 6:
Typ. channel reverse characteristics

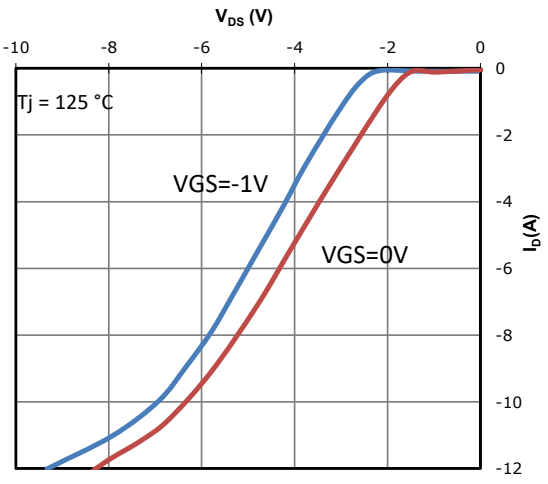


Fig 7:
Typ. channel reverse characteristics

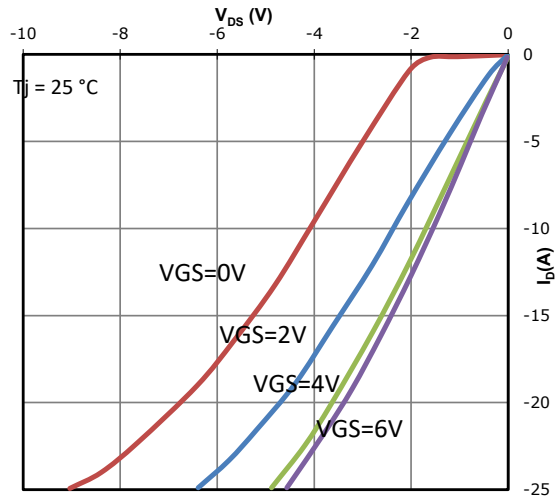


Fig 8:
Typ. channel reverse characteristics

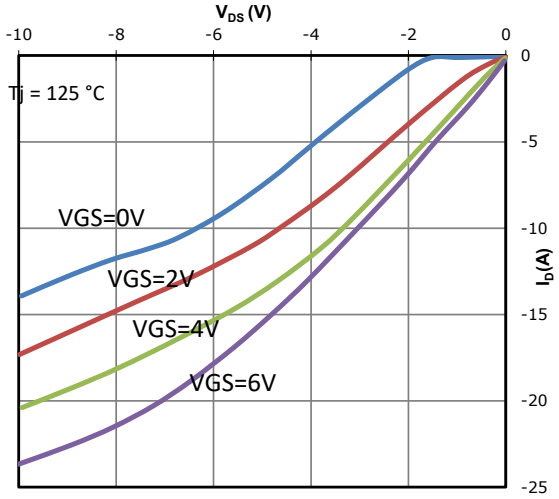


Fig 9: Typ. Transfer Characteristics

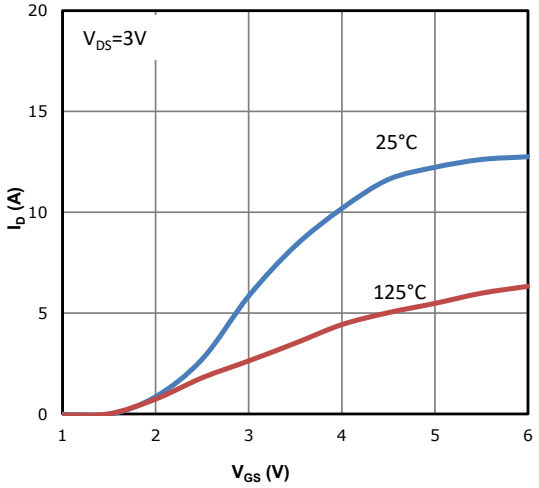


Fig 10: Typ. Gate-to-Source leakage

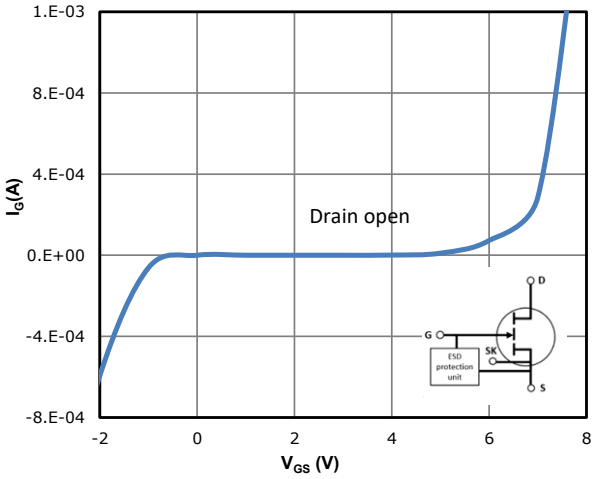


Fig 11:Drain-source leakage characteristics

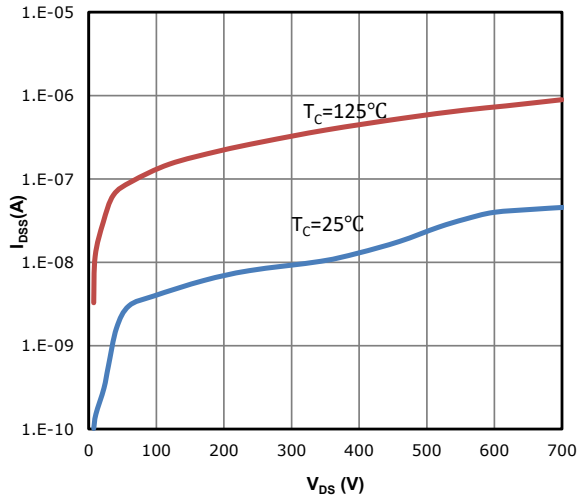


Fig 12: Vgs(th) vs. Temperature

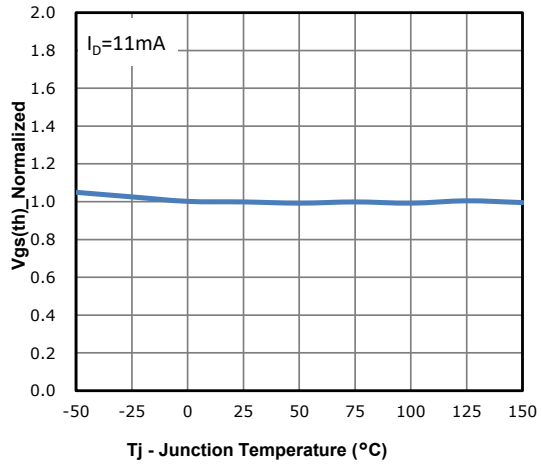


Fig 13: Rds(on) vs. Temperature

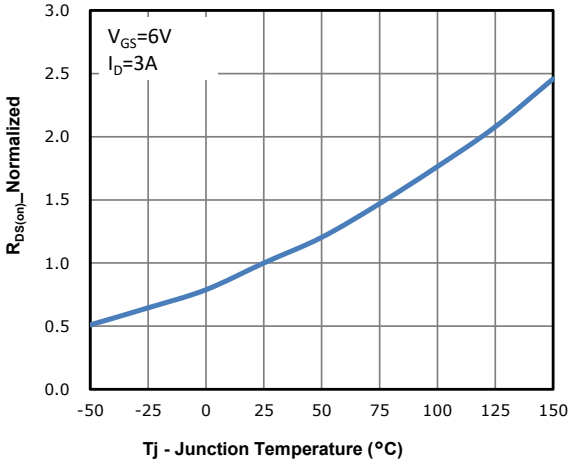


Fig 14: Power Dissipation

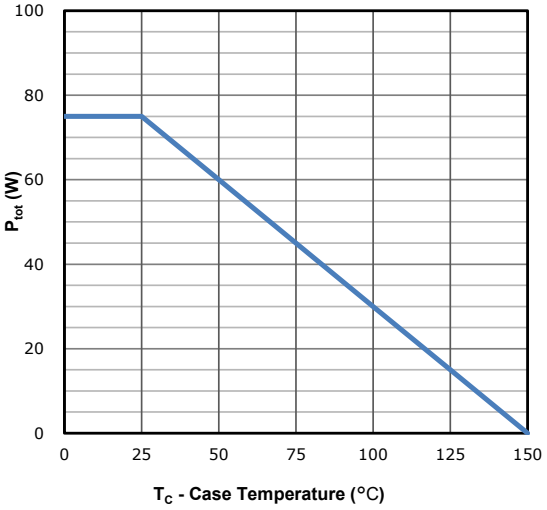


Fig 15:
Max. Transient Thermal Impedance

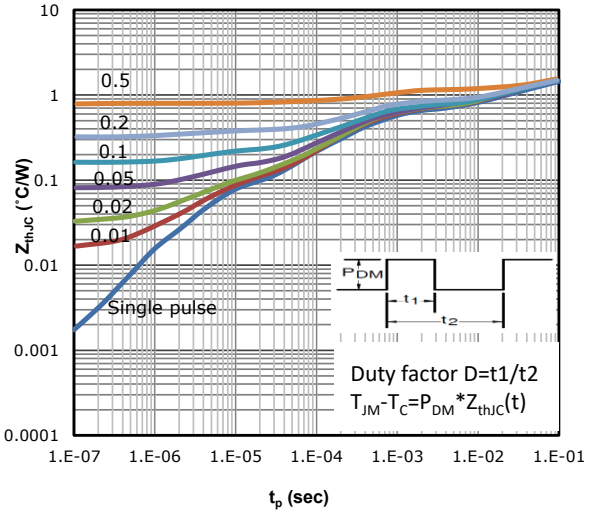


Fig 16: Safe Operating Area

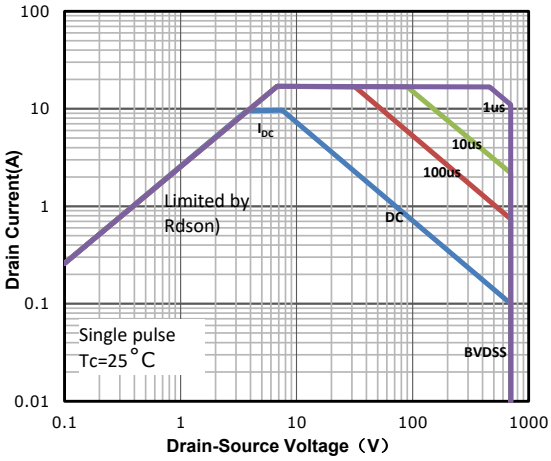


Fig 17: Safe Operating Area

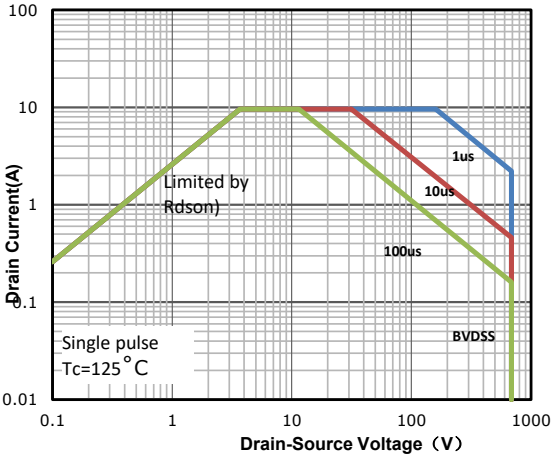


Fig 18: Gate ChargeCharacteristics

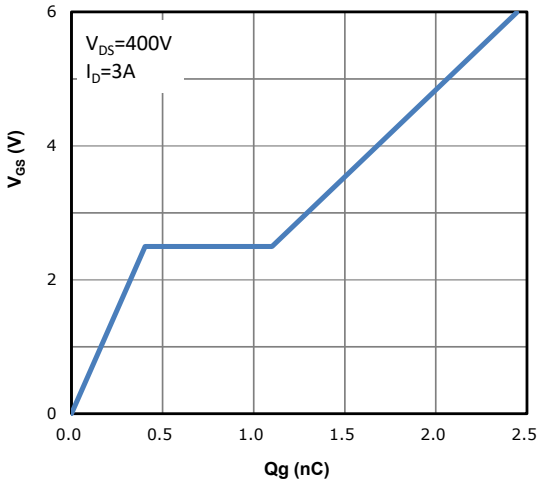


Fig 19: Capacitance Characteristics

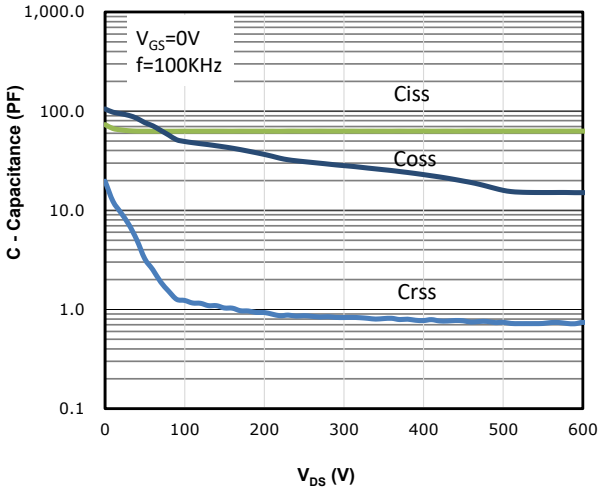


Fig 20: Typ. output charge

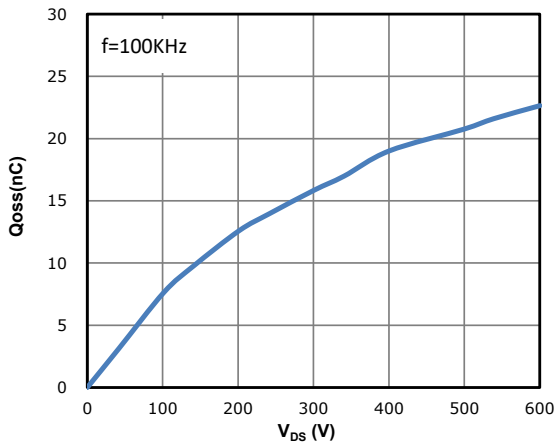
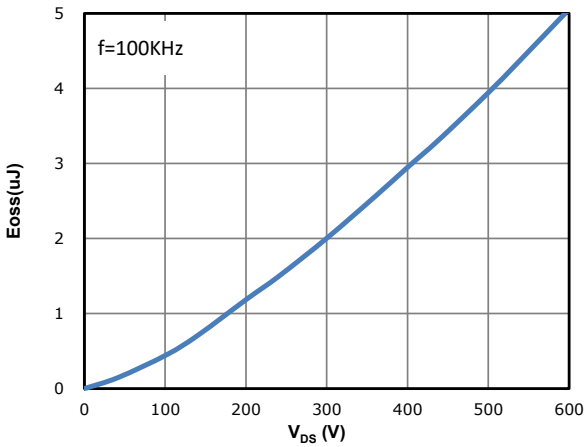
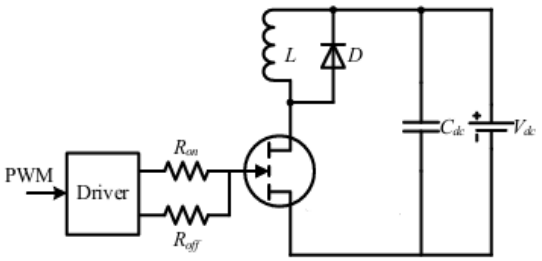


Fig 21: Typ. C_{OSS} stored Energy



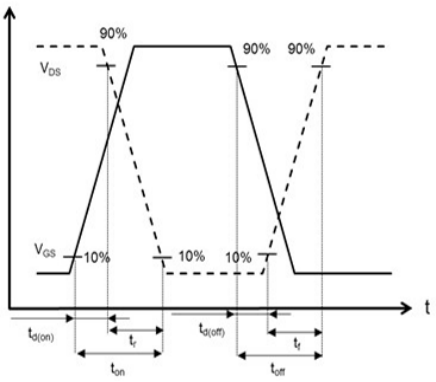
Test Circuit & Waveform

Fig 22：Typ.Switching time with inductive load

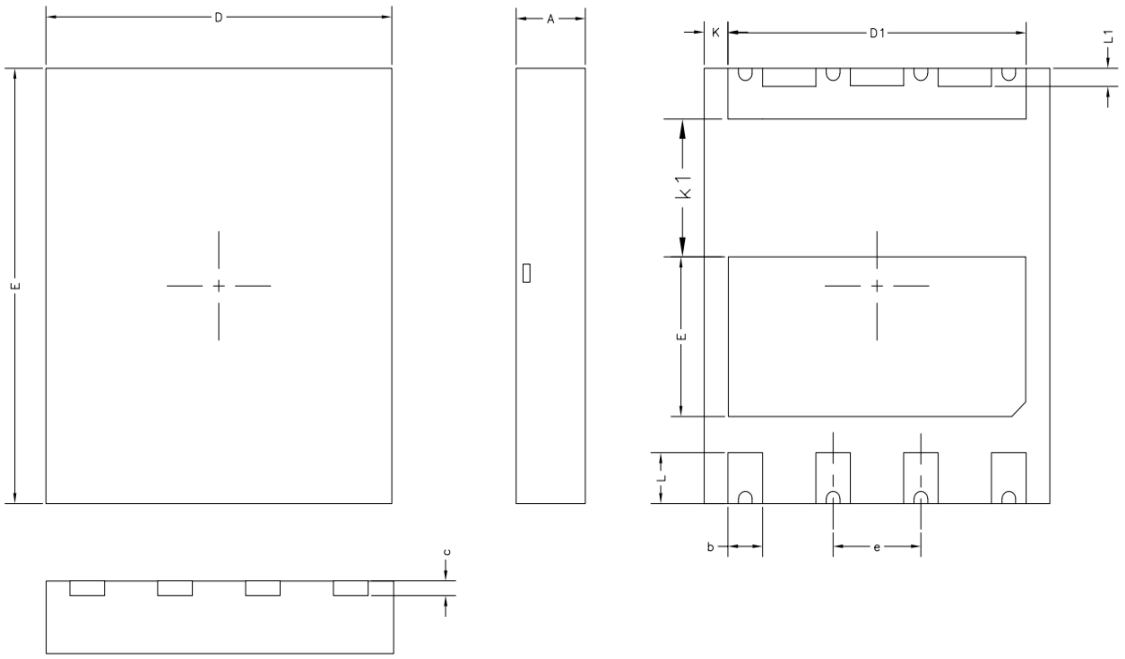


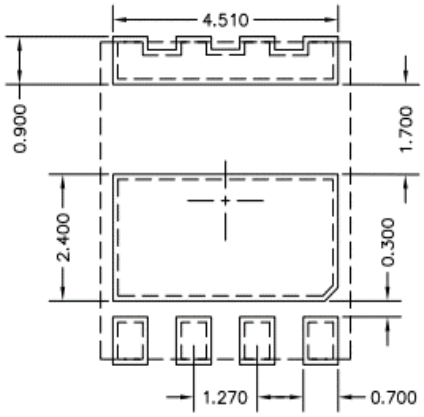
VDS=400V，ID=6A,L=318μH，
VGS=6V，Ron=10Ω，Roff=2Ω

Fig 23：Typ.Switching times waveform



Package Outline: DFN5X6





RECOMMENDED LAND PATTERN

SYMBOLS	DIMENSIONS MILLIMETERS		
	MIN	NOR	MAX
A	0.9	1.00	1.10
b	0.4	0.5	0.6
C	0.18	0.203	0.25
D	4.85	5	5.15
D1	4.16	4.31	4.46
E	5.85	6	6.15
e	1.27bsc		
L	0.55	0.7	0.85
L1	0.15	0.25	0.35
K	0.325	0.345	0.355
K1	1.70	1.90	2.10

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