

Features

- Uses PingWei advanced PerfectMOS5 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Excellent Low Ciss
- Qualified according to JEDEC criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterruptible Power Supplies)

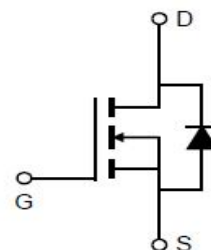
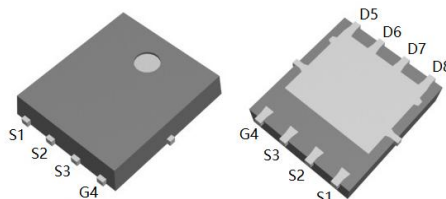


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	60V
$R_{DS(on)}@10V$ typ	1.3mΩ
I_D	209A

DFN5x6



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWC015N06ES	C015N06ES	DFN5*6	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	60	V
Continuous drain current	I_D	209	A
$T_C = 25^\circ\text{C}$ (Silicon limit)		300	
$T_C = 25^\circ\text{C}$ (Package limit)		132	
$T_C = 100^\circ\text{C}$ (Silicon limit)		22	
$T_a = 25^\circ\text{C}$			
Pulsed drain current ($T_C = 25^\circ\text{C}$, $t_p = 100\mu\text{s}$)	$I_{D \text{ pulse}}$	836	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $V_{ds}=50\text{V}$)	E_{AS}	256	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	125	W
$T_C = 25^\circ\text{C}$		1.3	
$T_a = 25^\circ\text{C}$			
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	R _{thJC}	-	-	1.0	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	R _{thJA}	-	-	93	°C/W	-

Electrical Characteristic (at T_j = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250uA
Gate threshold voltage	V _{GS(th)}	2	-	4	V	V _{DS} =V _{GS} , I _D =250uA
Zero gate voltage drain current	I _{DSS}	-	0.05	1	μA	V _{DS} =100V, V _{GS} =0V T _j =25°C T _j =150°C
Gate-source leakage current	I _{GSS}	-	±10	±100	nA	V _{GS} =±20V, V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	1.3	1.5	mΩ	V _{GS} =10V, I _D =50A
Transconductance	g _{fs}	-	92	-	S	V _{DS} =5V, I _D =50A

Dynamic Characteristic

Input Capacitance	C _{iss}	-	5339	-	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
Output Capacitance	C _{oss}	-	1274	-		
Reverse Transfer Capacitance	C _{rss}	-	128	-		
Gate Total Charge	Q _G	-	77	-	nC	V _{DS} =30V, I _D =50A , V _{GS} =10V
Gate-Source charge	Q _{gs}	-	27	-		
Gate-Drain charge	Q _{gd}	-	10	-		
Turn-on delay time	t _{d(on)}	-	25	-	ns	V _{GS} =10V, V _{DD} =11.7V, R _{G_ext} =2.5Ω, I _D =50A
Rise time	t _r	-	20	-		
Turn-off delay time	t _{d(off)}	-	38	-		
Fall time	t _f	-	11	-		
Gate resistance	R _G	-	0.8	-	Ω	V _{GS} =0V, V _{DS} =0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.83	1.2	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Continuous Forward Current	I_S	-	-	209	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	836	A	$TC = 25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	88	-	ns	$I_F=8A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	258	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

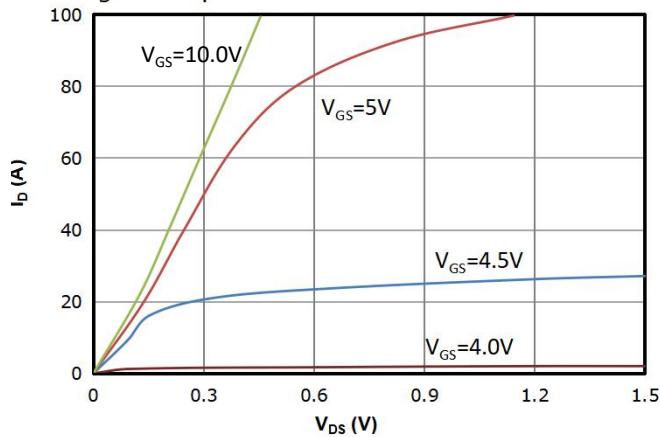


Fig 2: Transfer Characteristics

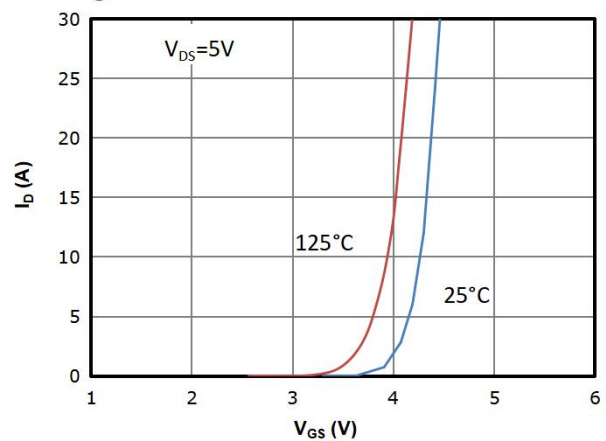


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

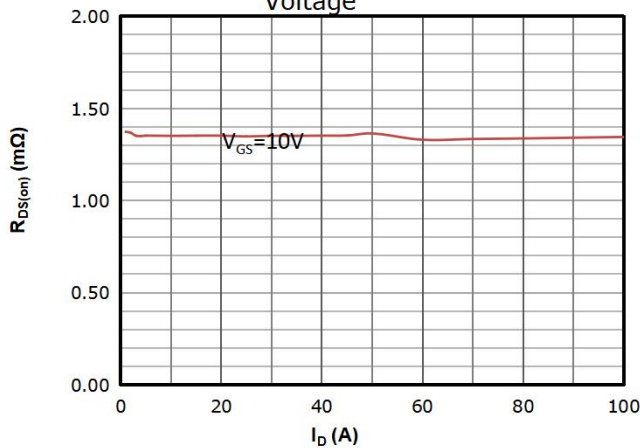


Fig 4: $R_{DS(on)}$ vs Gate Voltage

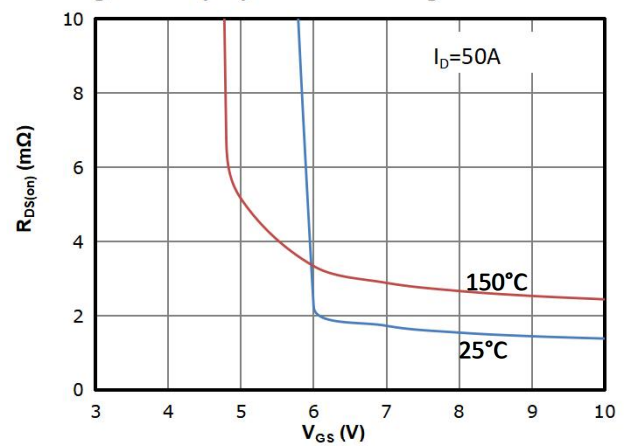


Fig 5: $R_{DS(on)}$ vs. Temperature

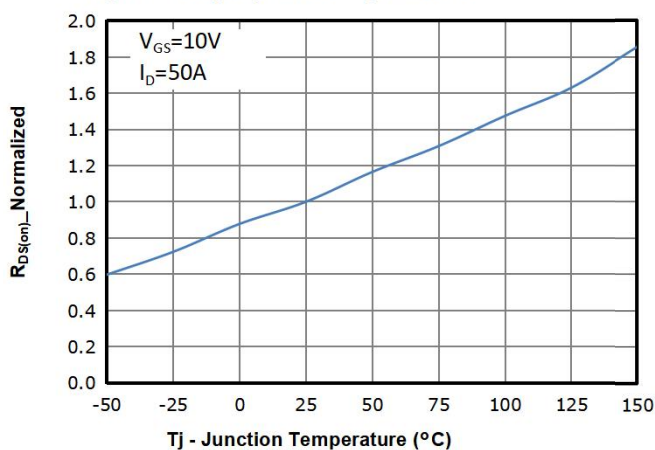


Fig 6: $V_{GS(th)}$ vs. Temperature

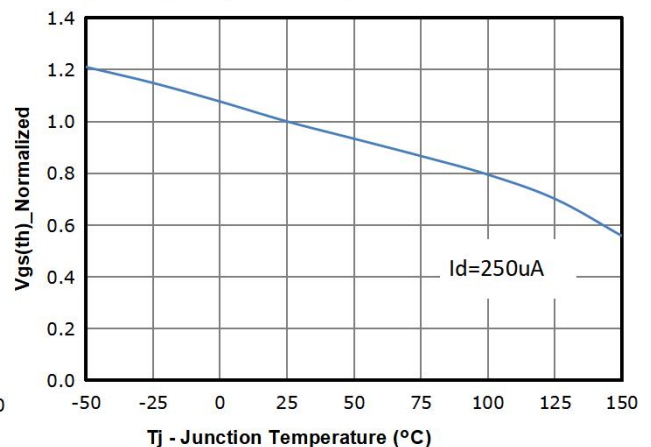


Fig 7: BVdss vs. Temperature

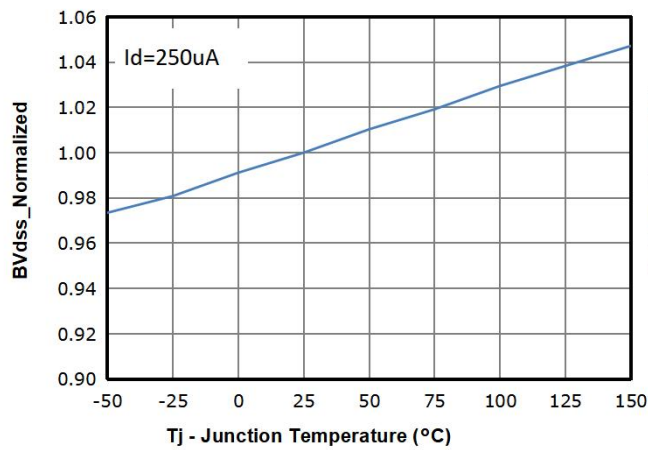


Fig 8: Capacitance Characteristics

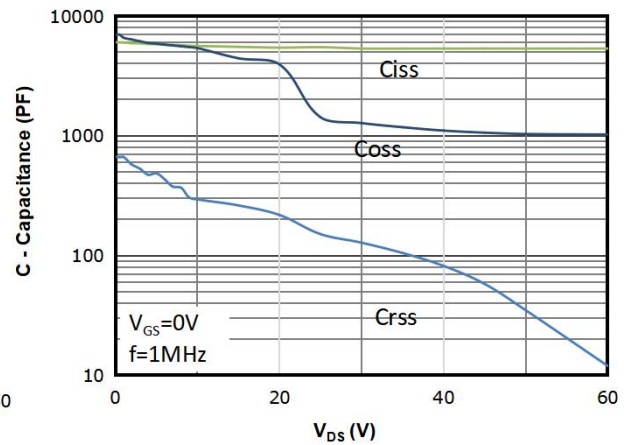


Fig 9: Gate Charge Characteristics

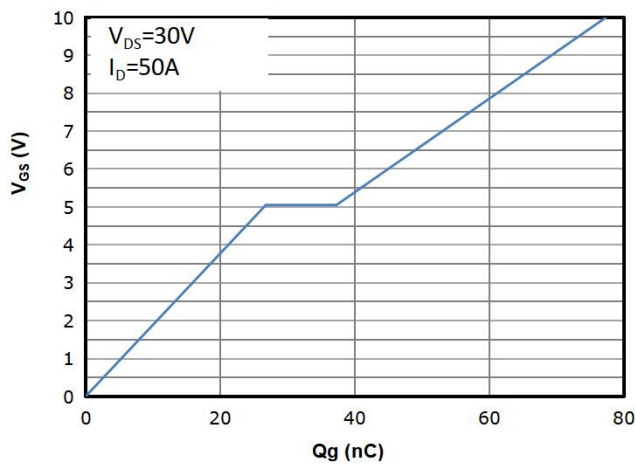


Fig 10: Body-diode Forward Characteristics

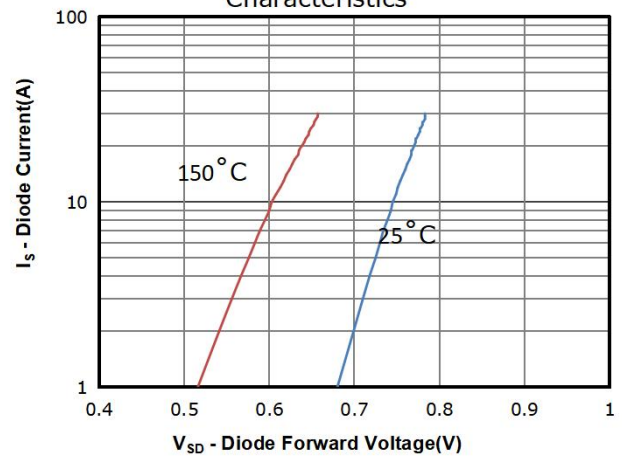


Fig 11: Power Dissipation

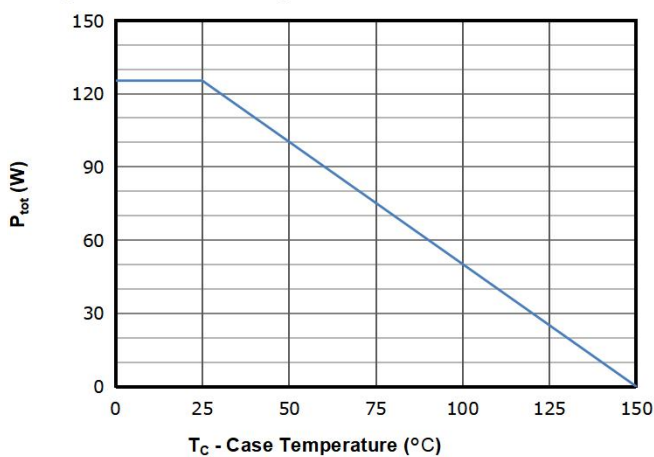


Fig 12: Drain Current Derating

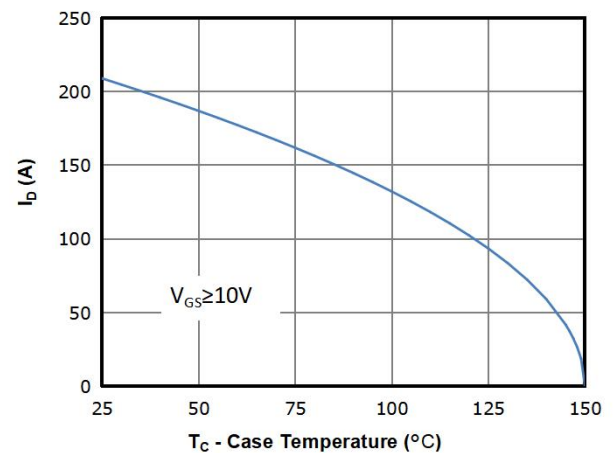


Fig 13: Safe Operating Area

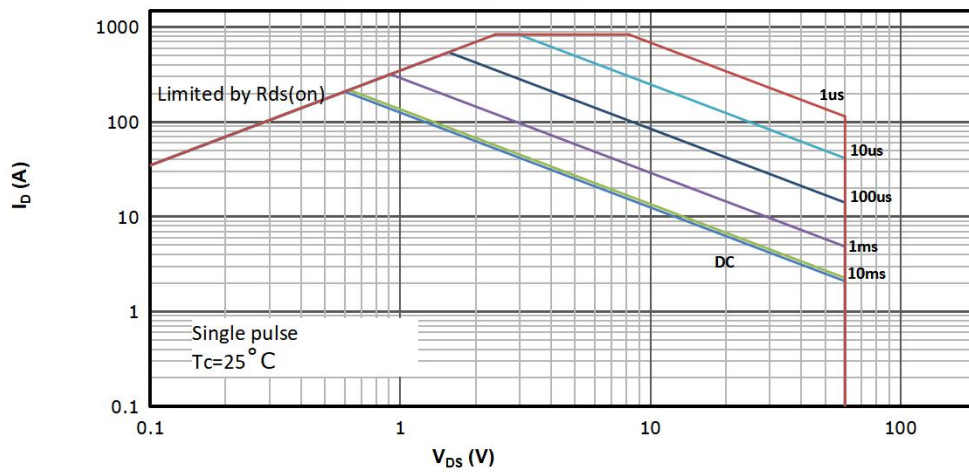
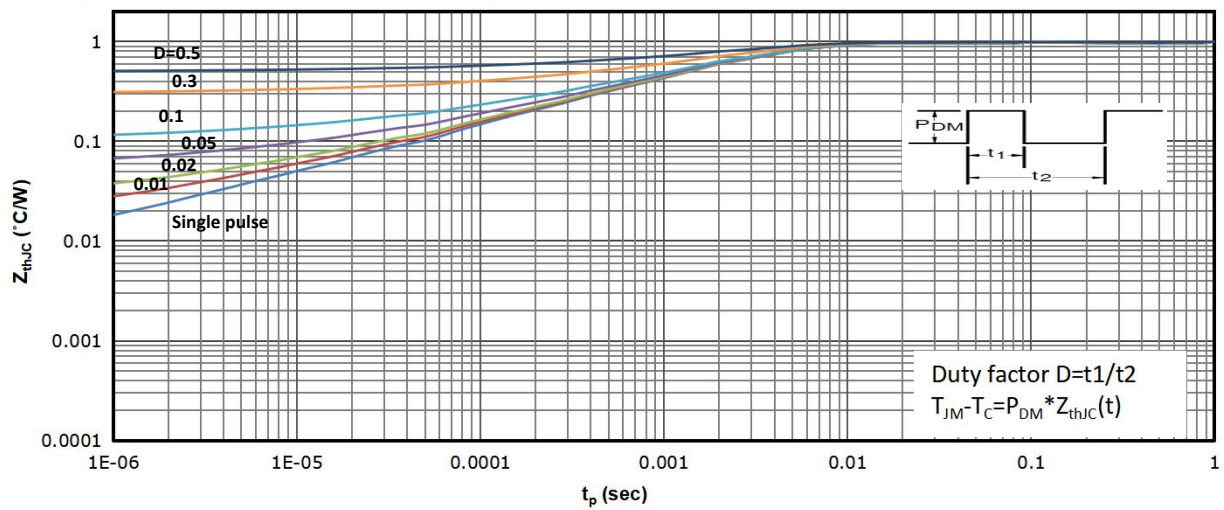
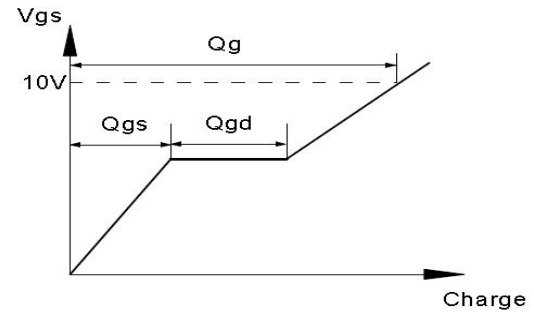
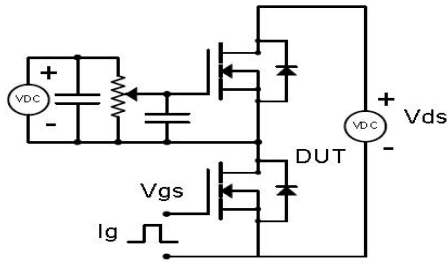


Fig 14: Max. Transient Thermal Impedance

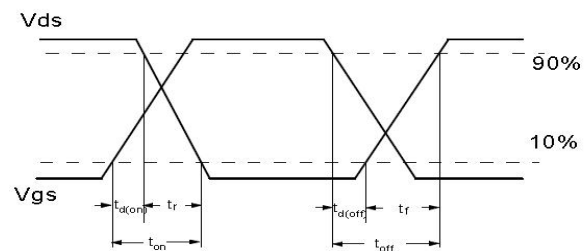
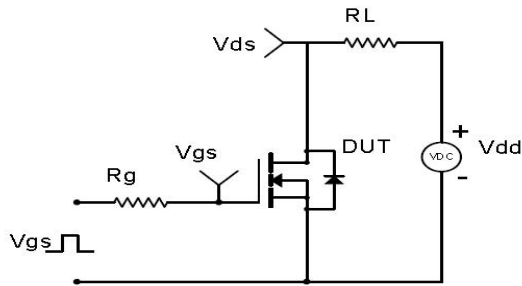


Test Circuit & Waveform

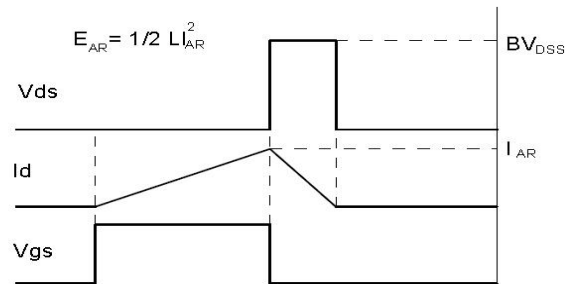
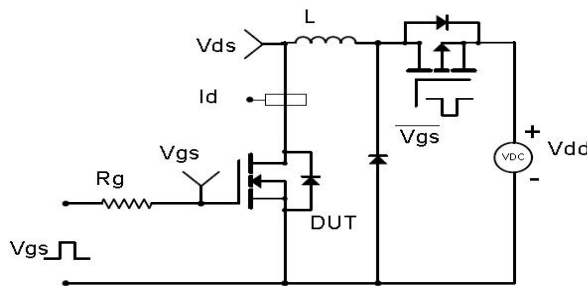
Gate Charge Test Circuit & Waveform



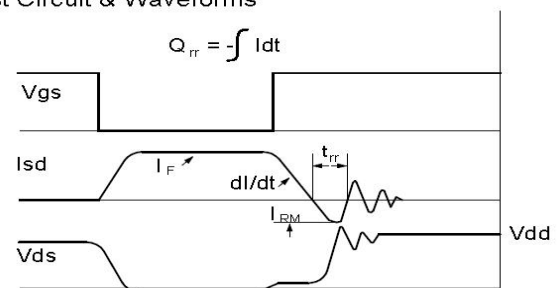
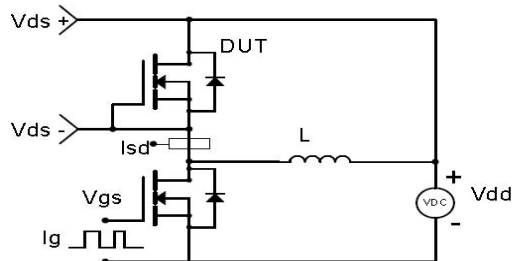
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

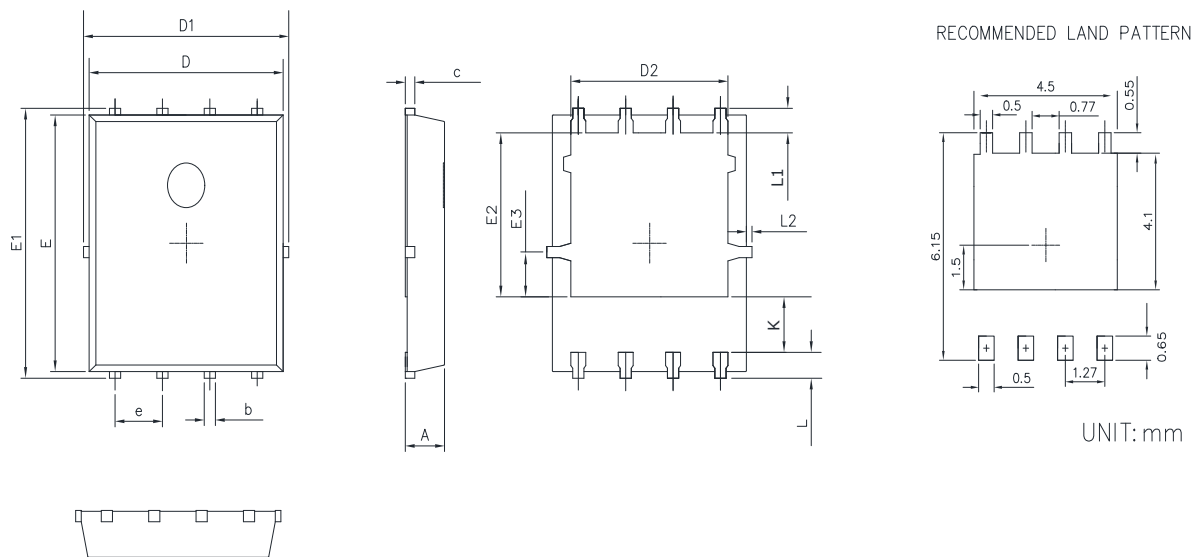


Diode Recovery Test Circuit & Waveforms





Package Outline: DFN5X6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.25	0.50	0.010	0.020
c	0.10	0.30	0.004	0.012
D	4.80	5.30	0.189	0.209
D1	4.90	5.50	0.193	0.217
D2	3.92	4.20	0.154	0.165
E	5.65	5.85	0.222	0.230
E1	5.90	6.20	0.232	0.244
E2	3.33	3.78	0.131	0.149
E3	0.80	1.00	0.031	0.039
e	1.27		0.050	
L	0.40	0.70	0.016	0.028
L1	0.65		0.026	
L2	0.00	0.15	0.000	0.006
K	1.00	1.50	0.039	0.059



Revision History

Revision	Date	Major changes
1.0	2023/1/4	Release of Formal Version.

Disclaimer

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

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